**Smartare Elektroniksystem**
ELECTRONIC COMPONENTS & SYSTEMS

# Reliability Assurance of Soldered Printed Board Assemblies

## Revision management

This version of the handbook, "Reliability assurance of soldered printed board assemblies" (published 2024) will replace the first edition "Tillförlitlighet hos mönster- och kretskort" (Published in 2017).

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# Foreword

**Smarter Electronic Systems is a strategic innovation program** within the frame of Vinnova's, Formas' and The Swedish Energy Agency's joint venture regarding strategic innovation areas. The program's objective is to support Swedish industry concerning world class sustainable development and competitiveness. In the program agenda three main challenges were highlighted as the most important in order to achieve the requirements of the future. These three were: leading edge competencies, supply and management of competencies, and efficient value-chains. For each challenge, a council was appointed. In the scope for the council regarding efficient value-chains, the work on handbooks were initiated. The first handbook, "Smartare Elektronikhandboken", was first published in 2017, version 2.0 came a couple of years later and has received great appreciation and use within the industry and in education. The Smarter Electronics Handbook has been followed by additional handbooks of which this publication, the Smarter Power Electronics Handbook, is one. The handbooks are maintained by the Swedish Electronics Trade association. This publication, Reliability assurance of soldered printed board assemblies, has been written by Per-Erik Tegehall in cooperation with the participants in the research projects and published by Smarter Electronic Systems.

This handbook, in combination with the "Smartare Elektronikhandboken" (The Smarter Electronic Handbook), and the following handbooks enables effective knowledge transfer between participants cooperating to develop electronic products which are both competitive and reliable.

We hope that you will find the handbook usable in your daily work. It contains the result from many years of research within the area of reliable PCBs and solder joints.

Please feel free to distribute the handbook among your suppliers and customers!

**The handbook is downloadable from:**

www.smartareelektroniksystem.se and www.svenskelektronik.se

# Preface

**The objective of this report is to provide basic knowledge of failure mechanisms that affect the reliability of soldered printed board assemblies and how reliability can be assessed and verified using a physics-of-failure based methodology.**

The document is largely based on results from research projects carried out at RISE (and at previous research institutes that now form part of RISE) for which I have been the project manager. Therefore, some failure mechanisms are covered in more detail than other failure mechanisms.

Most of the results originate from three research projects. These were with references given to open reports from the projects:

- "Lead free electronics for demanding automotive applications" (Vinnova dnr 2010-02853), 2011-2014 [1, 2, 3].
- "Requirements specification and verification of environmental protection and life of solder joints to components – TFP1" (Vinnova dnr. 2015-01420), 2015-2017 [4, 5, 6, 7, 8, 9, 10].
- "Reliability of PCB assemblies in products with high reliability requirements during a long expected life – TFP2" (Vinnova dnr. 2020-02863), 2020-2023 [11, 12, 13, 14, 15, 16].

The first project was funded by the FFI programme "Vehicle Development". The two other projects were performed within the strategic innovation program "Smartare Elektroniksystem", a joint venture of VINNOVA (Swedish Governmental Agency for Innovation Systems), Formas (The Swedish Research Council for Environment, Agricultural Sciences and Spatial Planning) and Energimyndigheten (Swedish Energy Agency).

# 1. Introduction

**At the same time as there are demands/expectations from customers that the reliability of electronic products should be constantly improved, many ongoing changes entail an increased risk of reduced reliability.** Examples of the most important changes are:

- New technologies are implemented more and more rapidly in new products. It may be to improve functionality, lower manufacturing costs or due to legal requirements.
- New technologies are developed primarily for consumer products with a short life expectancy and a mild operating environment.
- Product cycles are getting shorter and shorter, which places demands on an increasingly shorter "Time-to-Market", but it may also cause components to become obsolete after a short time on the market.
- More and more products are portable and/or used in harsher operating environments.
- More parties are involved in the product development chain due to the extensive out-sourcing.
- There is a strong pressure to minimise costs at all stages of the product development chain.

It is obvious that if you manufacture electronics with high reliability requirements and a long-life expectancy, or electronics that are used in harsh environments, you need to be aware of how these changes affect reliability in order to not risk decreased reliability, or delays in product launch.

The traditional way of working to ensure quality of electronic hardware is to design, manufacture and test according to “how-to” standards and guidelines, but the rapid development of new technologies have made it impossible to update these documents at the same pace. Another problem is that many standards are based on "best manu-facturing practice". That is, they are based on experience of mature technologies. Therefore, there is always a risk that requirements in standards and guidelines are not sufficient, or that they are not even relevant, when implementing new technologies.

Consequently, it is important to set relevant reliability requirements when procuring printed circuit boards[1] (PCBs) and printed board assemblies (PBAs) to ensure that the products will be reliable during the expected lifetime. This applies especially if you have products with high reliability requirements, a long-expected life and/or a harsh operating environment. An exception might be if you have a long relationship with your PCB and/or PBA suppliers and trust

[1] In IPC documents, “printed circuit boards” are often referred to as just “printed boards”.

them to deliver products with high reliability. It is not as important then, but even then, it may be advisable that you have specified reliability requirements should reliability problems arise.

Hence, due to the fast implementation of new technologies, ensuring reliability requires a different way of working than the traditional standard-based way of working. It requires knowledge of the failure mechanisms that may affect the reliability and how the reliability may be assessed and verified. Therefore, this new way of ensuring reliability is usually called "physics-of-failure based", "performance based" or "knowledge based". Standards for reliability programmes based on this approach have been developed by IEEE, SAE and GEIA [17, 18, 19].

Although meeting requirements in traditional standards may not be sufficient to ensure that a product will be reliable, it is a good starting point for ensuring reliability. Failure to meet these requirements carries a high risk of poor reliability.

In conclusion, ensuring reliability of soldered assemblies is a huge challenge, especially if new technologies are used to produce the assemblies and/or if they will be used under harsh conditions. Ensuring reliability according to the "new" reliability standards will require deep knowledge of the failure mechanisms that may affect the reliability of electronic hardware and how reliability can be assessed and verified. For many companies it will be difficult to acquire and maintain such knowledge. As I see it, they have three options.

**Option 1:** Use only mature technologies known to be reliable. This may mean, for example, that you may not be able to use new components with improved performance or lower price. Also, you should only use suppliers that you know from experience can deliver products with high quality. This means, for example, that you may not be able to switch to a new supplier that offers a lower price if you have no experience that he can deliver products that meet your reliability requirements.

**Option 2:** You can hope for the best and only require that requirements in applicable standards are met. If you are lucky, and in most cases you will be, you will have no serious reliability problems and have saved a lot of efforts and money. Without doubt, a very attractive option. The downside is that there is a higher risk of serious reliability issues.

**Option 3:** You will acquire and maintain the knowledge necessary for ensuring reliability per reliability programme standards (will be described later). Thereby, you will greatly reduce the risk for serious reliability problems. It will also be a good marketing strategy to be able to claim that the reliability has been ensured by following these reliability programme standards. In fact, many OEM companies will likely in the near future require that reliability is ensured by following these reliability programme standards.

Basically, ensuring reliability is a question of risk management. What risk are you willing to take to decrease costs and time to market? Whichever option you choose, it should be an informed decision based on an understanding of the risks. Even if you choose options 1 or 2, you can benefit from having a basic knowledge of the failure mechanisms that might affect the reliability of your products. For example, if you get a product change notification from a manu-facturer of a BGA telling you that the moulding compound has been changed to improve the

reliability of the component, do you know the risk it poses to you? (Answer in section about moulding compounds)

From the 1960s to the 1980s, the reliability of new technology was mainly assured by U.S military standards. These assured robust electronic products and failures were mainly caused by manufacturing defects resulting in "infant mortality" failures. These usually occurred fairly soon in the field and in most cases only a fraction of manufactured products was affected. Therefore, the costs of failures were usually not too high. Today, when new technology is primarily developed for the commercial market, it is a much higher risk that failures will be caused by wear-out failure mechanisms. It may take 5-10 years or more before failures will occur in field. Also, all products produced during that interval may be affected by this reliability issue. Therefore, the costs may be extremely high, and in worst case scenario, it could bankrupt your business.

That happened to Takata Corporation, a previous major manufacturer of airbags [20]. Due to a defective propellant and a long period of aging, the airbags could inflate improperly and even send shrapnel into the occupant. To date, there have been 26 deaths and more than 400 injuries due to this problem in the United States. When the problem was discovered, there were already a very large number of airbags on the market, and it was not possible to identify which airbags might have the defect. Even though the failure level was only a few ppm, it led to the biggest recall of cars to date. A total of 67 million airbags have been recalled. Due to the extremely high costs for the recall, Takata filed for bankruptcy.

Although the reliability problem with the Takata airbags was not caused by electronics, it could just as well have been caused by a wear-out failure mechanism in electronic hardware.

The objective with this document is to describe what is needed to perform to ensure reliability using a physics-of-failure (PoF) methodology. It will describe the most important IPC standards for rigid printed circuit boards and soldered printed board assemblies that have a direct impact on the reliability of the final products and discuss the relevance of various quality requirements in these standards.

The physics-of-failure based methodology of assuring reliability will then be shortly described. Since this approach requires knowledge of the failure mechanisms that may affect the reliability of electronic hardware and how reliability can be assessed, important failure mechanisms will be described and how their impact on reliability can be assessed and verified.

Finally, results from research projects on this subject performed at RISE will be presented.

# 2. Shortcomings of standard-based methodology to assure reliability

**In order to ensure quality of PCBs and PBAs, primarily standards developed by the IPC are used globally**. As previously mentioned, most of these standards are based on "best manufacturing practice". For soldered PBAs, the standard IPC J-STD-001, Requirements for Soldered Electrical and Electronics Assemblies, applies [21]. IPC has also produced a workmanship standard for PBAs called IPC-A-610, Acceptability of Electronic Assemblies [22]. The latter standard contains mainly interpretations of the requirements in J-STD-001, but also some additional requirements. In another IPC standard, J-STD-012 [23], it is stated that "*Meeting criteria in J-STD-001 and IPC-A-610 does not assure reliable solder connections, only quality solder connections*". Furthermore, in principle, all requirements for solder joints in these standards are based on visual inspection of the solder joints. There are no requirements of testing to verify the reliability of the solder joints. Therefore, compliance with the requirements in the two standards for soldered printed board assemblies does not assure that the solder joints will be reliable in field conditions, only that the visual requirements of the standards have been met. Hence, it is up to a user of the standards to assess whether the requirements are relevant and sufficient. One might think that this should be clearly pointed out in the standards, but that is not the case. It is taken for granted that users of the standards are aware of this.

The development of new types of components has mainly taken place to improve functionality and/or to lower manufacturing costs. Often, this has taken place at the price of a shorter life of the solder joints. In the mid-nineties, ball grid array (BGA) components began to be used. Since the entire connections between components and PCBs for these components consist of solder, you get a shorter service life for these compared to components equipped with leads such as quad flat packages (QFPs) where the leads act as relief springs. As the pitch has since then decreased for BGA components, and the chip inside them has become larger, the life of the solder joints has gradually decreased. Today, BGA components with a pitch of 0.3-0.5 mm are common. All these changes increase the stress on solder joints when assemblies are exposed to changes in temperature or vibration. Consequently, solder joints to lead-less[2] components may have a life that is only a few percent of the life of solder joints to components having leads. Therefore, it may become a reliability problem even for products with a short life expectancy that are used in a mild operating environment. Another component type that has issues with solder joint life is quad flat no-lead (QFN) components. This is also a lead-less component where the entire connections between the component and a PCB consist of solder.

[2] The term lead-less will be used with the meaning having no leads whereas the term lead-free will be used with the meaning containing no lead (Pb).

Thus, using BGA and QFN components can result in insufficient life even if soldering of the components is perfectly executed and the solder joints meet all requirements in applicable standards. Another problem with J-STD-001 and IPC-A-610 for these component types is that the standards mainly include visual inspection requirements of the solder joints. Since solder joints to BGA and QFN components are completely or partially located underneath the components, they are very difficult to inspect visually. X-ray microscopy can provide some information about the quality of the solder joints, but several types of common defects are difficult to detect even using X-ray microscopy.

Shorter service life of solder joints is an example of how new technologies have led to decreased reliability, but there are also other failure mechanisms that can have a negative impact on reliability. Not least, this applies to electronics with different types of sensors, which can be significantly more sensitive to various factors in the operating environment than traditional printed board assemblies.

# 3. Impact of outsourcing on reliability

**In 2013, the IPC published a cleanliness guideline for printed circuit board manufacturers, IPC-5703, Cleanliness Guidelines for Printed Board Fabricators [24].** In the introduction to the standard, it is noted that individuals who are responsible for assessing the quality of incoming printed circuit boards have lamented the fact that the cleanliness of PCBs is often an unknown quality parameter, many times with undesirable results, at many work meetings for IPC's standardisation groups. It was concluded that this is often due to a lack of knowledge on the part of the PCB manufacturer, but it is also caused by the fact that the industry has pushed the margins to such low levels that the PCB manufacturers cannot afford to keep "*experienced process professionals*".

There is also a great risk that this leads to PCB manufacturers reducing their costs by, for example, using drills and surface treatment baths longer than they should, using materials that have become too old or by not performing quality controls to the extent they should. There are many ways that you can reduce your costs that may reduce the quality of PCBs.

Therefore, it is important that you have specified reliability requirements when procuring especially PCBs, but you ought to have them also when procuring PBAs. Not having specified reliability requirements is like buying a pig in a poke. It can be very difficult and expensive to find out the cause of reliability problems afterwards. In IPC-5703 it is concluded that "*Tracing field failures to the cleanliness of incoming bare boards is often exorbitant of time and cost. What may only be a difference in pennies in a printed board fabrication process can cost an assembler hundreds of thousands of dollars to track down*".

# 4. Quality versus reliability

**Although almost all companies have some form of quality policy, they may have a wrong focus to ensure that the products will be reliable.** What often creates misunderstandings is that most standardisation organisations develop standards to ensure *quality* of products, but they have a definition of quality that does not include ensuring reliability.

A common difference in the definition of the terms "*quality*" and "*reliability*" used by most standardisation organisations is stated in "The Electronic Packaging Handbook" [25]:

*"A quality product will be defined as one that meets its specifications during the manufacturing and testing phases prior to shipment. This is different from reliability, which can be defined as a product meeting its specifications during its expected lifetime."*

With this definition of quality, the meaning of ensuring a product's quality becomes only to ensure that requirements in applicable specifications and standards are met. If it turns out that the requirements are not relevant or sufficient to ensure that the product will be reliable during operation, then by definition the quality requirements for the product have still been met.

For products manufactured using proven technologies, it is often enough to meet the requirements of the standards to assure that they have sufficient reliability. But the newer technology you use, the larger the risk that it will not be sufficient to meet the requirements of standards. This applies especially if the product has a long-expected life in a harsh operating environment with high reliability requirements. For these products, it may be necessary to supplement the requirements in standards with additional requirements.

However, the extensive outsourcing of PCB and PBA manufacturing over the past 25 years combined with a lack of adequate specification of reliability requirements has led to that many are experiencing reliability problems even with common technologies, especially for printed circuit boards.

See reference 1 for a more extended discussion of this topic.

# 5. General about IPC standards

**IPC has developed a large number of standards for PCB and PBA manufacturing. A list of their standards can be found at http://www.ipc.org/4.0_Knowledge/4.1_Standards/SpecTree.pdf**

The majority of these standards are also listed in the "IPC CHECKLISTA för produktion av Rigida PCBA's" developed by Lars Wallin in collaboration with "Svensk Elektronik" [24]. This checklist is in Swedish.

## 5.1 Classification

**End products have been divided** into three general classes which reflect differences in manufacturing possibilities, complexity, functional performance requirements and control frequency (inspection/test). One should be aware that there may be overlap between classes for a piece of equipment. A user and a manufacturer must agree on which class the product belongs to and should be stated in the purchase documents for both PCBs and PBAs.

### 5.1.1 IPC Class 1

General electronic products — Includes consumer products and some computer and computer peripherals suitable for applications where cosmetic imperfections are not important and the major requirement is function of the completed printed board.

### 5.1.2 IPC Class 2

Dedicated service electronic products. Includes communications equipment, sophisticated business machines, instruments where high performance and extended life are required and for which uninterrupted service is desired but not critical. Certain cosmetic imperfections are allowed.

### 5.1.3 IPC Class 3

High reliability or harsh operating environment electronic products. Includes the equipment and products where continued performance or performance on demand is critical. Equipment downtime cannot be tolerated and must function when required such as in life support items or flight control systems. Printed boards in this class are suitable for applications where high levels of assurance are required and service is essential.

Many requirements in IPC standards are default requirements, i.e. they generally apply unless otherwise agreed, while other requirements are AABUS requirements (As Agreed Between User and Supplier). The latter means that the user and manufacturer must agree on what applies regarding these requirements and that this must be written in procurement documents.

# 6. IPC standards for quality assurance of PCBs and soldered PBAs

## 6.1 Standards for printed circuit boards

### 6.1.1 IPC-6011 - Generic Performance Specification for Printed Boards

IPC-6011 [27] contains general quality requirements for printed boards. More specific requirements for different types of printed boards can be found in separate standards, of which only the one for rigid printed boards, IPC-6012 - Qualification and Performance Specification for Rigid Printed Boards [28], will be covered here. A related standard is IPC-6013 - Qualification and Performance Specification for Flexible/Rigid-Flexible Printed Boards [29]

IPC-6011 states that "*Printed boards furnished under this specification shall meet or exceed all the requirements of the specific class of this specification as required by the procurement documentation*". Furthermore, the procurement documentation must specify specific exceptions, variations, additions or conditions to the standard that the buyer has, and special tests required and frequency of these.

The PCB manufacturer must be able to demonstrate to the customer an assessment of their capability to manufacture PCBs. It is pointed out that "*there is no minimum level of Qualification Assessment Verification required by this specification*". Thus, it is up to the buyer to judge whether the capability evaluation is sufficient for his needs.

It is also required in IPC-6011 that the PCB manufacturer must have a "*Quality Assurance Program*" (type ISO 9000), a process control system and that all materials used must meet the requirements of applicable standards. He must be able to explain to the customer how the process control system is structured and how he ensures that the materials used meet the requirements of applicable standards.

### 6.1.2 IPC-6012 - Qualification and Performance Specification for Rigid Printed Boards

The requirements in IPC-6012 [28] are intended to supplement the requirements of IPC-6011 with specific requirements for rigid printed boards. IPC has also published a supporting document, IPC-A-610 [30], which contains figures, illustrations and photographs that can aid in the visualisation of externally and internally observable acceptable/nonconforming conditions. It may be used in conjunction with IPC-6012 for a more complete understanding of the recommendations and requirements.

Table 4-3 in the standard contains a compilation of parameters that must be verified during *acceptance testing* and how often these tests must be done. In total, there are 63 parameters that are listed, excluding tests of various constituent materials. The extent and frequency of testing is determined by the IPC class chosen and the batch size. Several of the requirements are AABUS requirements. These must be specified in the procurement document if they are to apply. If no requirement specification is specified in the procurement document, there is a list

in IPC-6012 of default requirements that apply. The verification of the parameters must either be done on the ordered PCBs or on specially designed test coupons that are manufactured at the same time as the PCBs. IPC has developed test coupon designs that can be used for this. The scope of the verification will of course have a directimpact on the price of the PCBs. Therefore, it is important not to state a higher class than necessary. You can also minimise the number of evaluations required in the purchase document if you are prepared to take the risk of poorer reliability (depending on your reliability requirements and past experience with the PCB manufacturer).

Many of the parameters are easy to verify, such as verifying that dimensional requirements are met. Others are more complicated to verify. Below are some examples of parameters that often cause reliability problems and for which it may therefore be important to have specified reliability requirements (depending on what reliability requirements you have).

### Surface finish requirements (Table 3-3)

Problems with wetting of solder surfaces on PCBs is a frequently recurring problem. The choice of surface finish on solder pads has a major impact on storability and solderability. There are a large number of different surface finishes to choose from, all of which have their pros and cons. Regardless of which surface finish is chosen, the quality of the surface finish is the most important factor for good solderability. With poor quality of the surface finish, the solderability will be poor regardless of which surface finish is chosen. An important parameter for the quality is the thickness of the surface finish. Below are the thickness requirements for some of the most common finishes:

- ENIG (Electroless Nickel/Immersion Gold): Ni minimum 3.0 µm and Au minimum 0.05 µm (thickness above 0.125 µm may indicate a "*black pad*" defect).
- HASL (Hot Air Solder Levelling): Coverage and solderable.
- OSP (Organic Solderability Preservative), immersion tin and immersion silver: solderable.

OSP is a very thin organic coating that prevents oxidation of the copper surface.

### Base metallic plating depositions and conductive coatings (clauses 3.2.6 and 3.6)

Poor quality of plated through hole (PTH) platings is a common cause of electrical interruptions in PCBs. In order to verify the quality of hole plating, the standard requires that one verifies the thickness of the hole plating and also verifies the integrity of the hole plating after thermal stress. The thermal stress shall be performed on the PCBs (or test coupons) by one of the following three methods:

- Floating for 10 seconds in a solder bath at 288 °C.
- Simulated soldering cycles with a peak temperature of 230 °C (for PCBs to be soldered with SnPb solder).
- Simulated soldering cycles with a peak temperature of 260 °C (for PCBs to be soldered with lead-free solders).

Next, a number of PTHs must be micro-sectioned to verify the integrity of the hole platings after the thermal stress (different requirements for the different IPC classes).

### Solder mask cure and adhesion (clause 3.7.2)

The degree of curing of the solder mask on a PCB can have a major impact on the reliability of the PCB and is a common cause of poor quality. A conclusion in IPC-5703 is that: "*A partially cured solder mask is a nightmare condition as the mask becomes a sponge for subsequent process fluids. Present cleanliness test methods often cannot detect this problem*". However, curing the solder mask is a balancing act because "*Excessive thermal cure can turn the solder mask brown and brittle*".

Reasons for the solder mask not being fully cured can be, for example, that UV lamps have not been changed frequently enough (these age over time, resulting in reduced effect) or that the PCB has not undergone all the thermal steps that are usually carried out in PCB manufacturing.

Under clause 3.7.2 "Solder Mask Cure and Adhesion" it is required that "*Visual assessment of the cured solder mask coating shall not exhibit tackiness, delamination, or blistering*". However, this is far from a sufficient requirement to verify that the solder mask is sufficiently cured, which means that the standard does not have a relevant requirement to verify the curing of the solder mask.

### Cleanliness (clause 3.8.4)

As previously mentioned, IPC-5703 lists poor PCB cleanliness as a common cause of reliability problems. There are several clauses in the standard that concern cleanliness.

Clause 3.8.4 has requirements for "Moisture and Insulation Resistance". Special test coupons with two parallel conductors in each layer and on top of each other are used for this test. During the test, the conductors have 100 V DC polarising voltage applied at 85 °C and 85 % RH for one week. After finished exposure, the insulation resistance is measured between the conductors in each layer and between the different layers at room temperature. The purpose of the test is to verify that contamination in the inner layer and moisture absorption do not result in too low insulation resistance.

Under clause 3.9.1, “Cleanliness Prior to Solder Mask Application”, it is stated that if the board requires a permanent solder mask coating, the uncoated boards shall be within the allowable limits of ionic and other contaminants prior to the application of solder mask coating. The clause refers to a measurement method and acceptance value for ionic pollutants. The measurement method is called "resistivity of solvent extract (ROSE)" and the contamination level shall not be greater than 1.56 $\mu g/cm^2$ of sodium chloride equivalents

Cleanliness measurement for inner layers before lamination, as well as for the finished PCB, are AABUS requirements (clauses 3.9.2 and 3.9.3). If you want to require that the cleanliness shall be measured on inner layers and on the finished PCB, this must be stated in the procurement document. This applies to both method and acceptance requirements.

It is worth noting that in IPC-5703, it is stated that "*the use of ROSE for product acceptance is not a valid practice, even though it is commonly done in the industry*". The reason for this is partly that the measurement accuracy is poor and partly that there is no direct connection between the measured value and the reliability of a PCB. However, ROSE is a useful test method to check that purity does not change over time.

An alternative way to measure cleanliness on PCBs is to measure the effect of possible contaminants on the surface insulation resistance (SIR). This is an AABUS requirement in IPC-6012 (clause 3.10.8). It is specified how the SIR measurement should be performed and acceptance requirements, but with the proposed measurement method, the measurements are performed at too low temperature and humidity to be relevant. A better option is to test the SIR according to IPC-9202 [31] using mini coupons for SIR testing (described in the standard).

## 6.2 Standards for soldered printed board assemblies

### 6.2.1 IPC J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

The scope of IPC's standard J-STD-001 [21] is to describe materials, methods and acceptance criteria for producing soldered electrical and electronic assemblies. The intent is to rely on process control methodology to ensure consistent quality levels during the manufacture of products. It prescribes material requirements, process requirements, and acceptability requirements.

As previously mentioned, IPC has also produced a workmanship standard for PBAs called IPC-A-610, Acceptability of Electronic Assemblies [22]. The latter standard mainly contains interpretations of the requirements in J-STD-001, but also some additional requirements.

There are mainly three quality issues at assembly level that may have a large impact of the reliability of soldered assemblies. These are:

- Quality of solder joints.
- Cleanliness level of an assembly.
- Capability of applied coatings and encapsulations to provide environmental protection in harsh conditions.

#### Quality of solder joints

To assure quality of solder joints, the standard has requirements for materials and processes used in the manufacture of soldered assemblies including rework and repair processes. For all types of components, it has requirements of the maximum allowable displacement of the leads/ terminations on the components in relation to solder lands on the PCB. In addition, it has requirements on the appearance of the solder joints, in most cases visual requirements.

For area array components it is assumed that an inspection process is established to determine compliance to area array criteria. However, since this is not possible to achieve by visual inspection, except maybe for the outside row of solder joints, X-ray inspection needs to be used.

In addition to requirements on the appearance of the solder joints for ball grid array components, the standard has also requirements of the maximum allowable amount of voids in the solder joints. It should be less than 30 % of any ball in the X-ray image area. Design induced voids (e.g. caused by microvia-in-land) and plating process induced voids (e.g. micro voids) are excluded from these requirements. In such cases, the acceptance of the voids will need to be established between the manufacturer and user.

For bottom termination components (e.g. QFN/MFL components), the standard has no requirement for the thermal transfer plane since these are design and process related. For the solderable surface of a termination under the component, the requirement is that wetting is evident. For components that have continuous solderable surfaces on the sides, a toe fillet may form. However, the requirement for the toe fillet in the standard is "*Unspecified parameter or variable in size as determined by design*".

It is pointed out in the standard that for lead-less components, the prime parameter in determination of solder connection reliability is the solder fillet thickness defined as the distance from the top of the solder land on the PCB to the bottom of the termination on the component. From reliability point of view, a thick solder fillet is desirable. Nevertheless, the requirement in the standard for the solder fillet thickness for all lead-less components is only that wetting is evident. This includes ceramic resistors and capacitors.

As already discussed, the lifespan of solder joints, including fine-pitch BGA and QFN components, has decreased and it is impossible to make an assessment of their lifespan from a visual inspection of solder joints. Nevertheless, J-STD-1 does not have any requirements that the reliability of solder joints shall be tested and verified.

For commercial products with a relatively short life expectancy, the shorter life of solder joints to these components is not normally a problem, but can be a major problem for products with a long-life expectancy and severe operating environment. Therefore, specially dedicated documents have been developed for these component types [32, 33, 34]. These documents are not standards with specified requirements that can be referred to in procurement documents. Instead, the purpose with these documents is to "*provide useful and practical information to those who are considering implementation of the component types*". They describe various aspects that can affect reliability such as construction of the components, design of printed circuit boards and production processes for printed circuit board soldering. They also provide guidance on how to design relevant reliability tests for different applications. Thus, it is up to the user of the standards to assess what he needs to do to ensure reliability and what requirements he should place on assembly manufacturing (whether it is done in-house or if it is outsourced).

### Cleanliness of assemblies (Chapter 8)

Poor cleanliness of assemblies is a common cause of failure, especially in operating environments with high humidity. The most common cause of poor cleanliness is flux residues from soldering of the assemblies. Therefore, cleanliness of soldered assemblies is an important quality measure of assemblies.

For a long time, the cleanliness requirements in J-STD-001 were:

- Assemblies shall be free of foreign particles that are loose.
- Unless specified by the user, the manufacturer should specify a cleanliness designator that establishes the cleaning option and test for cleanliness. In the absence of a specified cleanliness designator, both sides of assembly shall be cleaned[3] and test for ionic residues shall be performed.

The default test for ionic residues was the same test as for PCBs (clause 3.8.4 in IPC-6012) with the same acceptance criterium of maximum 1.56 $\mu g/cm^2$ sodium chloride equivalents.

In 2018, Amendment 1 was added to revision G of IPC J-STD-001 [35]. The requirements in this amendment have now been included as a part of revision H of the standard [21].

In the amendment and revision H of the standard, the requirements for cleanliness verification have been tightened. Unless otherwise specified by the user, the manufacturer of class 2 and class 3 products shall[4] qualify soldering and/or cleaning processes that result in acceptable levels of flux and other residues. Rework processes shall be included. Objective evidence shall be available for review.

It is pointed out that the use of 1.56 $\mu g/cm^2$ sodium chloride equivalents value for ROSE testing, with no other supporting objective evidence, is not considered an acceptable basis for qualifying a manufacturing process.

However, it is not entirely clear what is meant by objective evidence, but essentially the following can be counted as objective evidence:

- If a manufacturer has been using a defined material set for many years, with no identified reliability issues related to flux residues, this should be considered as objective evidence. A proven track record on manufactured product with demonstrated field reliability should be considered as acceptable. No other testing should be required.
- If a manufacturer produces a product that meets the customer requirements and passes the customer-required product qualification testing, this may constitute objective evidence. The key consideration is whether the qualification test regimens which would show electrochemical failures. If it does not, it would not constitute objective evidence.

[3] It is possible to choose no surfaces to be cleaned.
[4] Shall means that it is a mandatory requirement.

- If an assembler is using a sole flux supplier, then vendor-produced compatibility information would be considered as acceptable objective evidence provided the assembler is using the fluxes to the flux vendor's recommended guidelines.

- If an assembler has evaluated material and process compatibility per IPC-9202 [31], or similar standards, this should be considered as acceptable objective evidence.

That is, qualification of a manufacturing process can be done both by testing functional products and by testing special test assemblies.

After a manufacturing process has been qualified, a process for ionic residue testing shall be established. That is a requirement for class 3 products but is also recommended for class 2 products. The manufacturer shall determine an objective sampling plan for measuring ionic residues of the process using ROSE or other methods as agreed between manufacturer and user. The sampling plan shall define test method, test frequency and upper control limit based on the results from process qualification and have objective evidence available for review. There is no stated requirement for sampling frequency except that once a year is not an acceptable frequency. Instead, it is stated that the most common sampling frequency in use today is sampling once per manufacturing shift.

Even if you can produce an assembly that is completely free from contamination, condensation of water on a biased assembly may cause a failure within a few seconds due to short circuits. Thus, meeting the criteria of IPC J-STD-001 in terms of cleanliness may not be sufficient to ensure reliable use in harsh conditions. Assemblies used in harsh conditions may need some type of protection against the operating environment.

### Capability of applied coatings and encapsulations to provide environmental protection (Chapter 10)

A possible solution is to use a hermetic casing (not covered in J-STD-001) but, for many who have tried this, it has ended up with water getting in but not out.

An alternative is to use a conformal coating (covered in J-STD-001). This is an organic material and therefore permeable for gaseous molecules including water molecules. Residues present on the PCB surface prior to the application of a conformal coating may absorb humidity from the environment and cause electrochemical migration or delamination of the coating. Therefore, the standard has a requirement that assemblies shall be clean before processing and that they after cleaning shall be handled in a manner that prevents contamination prior to processing.

This can be interpreted as cleaning is required to be carried out, even if it is not clearly stated. Nevertheless, many today coat assemblies manufactured using no-clean fluxes without cleaning before coating. If this is done, it should be kept in mind that any contamination added to the assemblies during manufacturing will remain on them when coating. Therefore, coating without prior cleaning requires very good process control to ensure that the assemblies are not contaminated at any process step. Apparently, J-STD-001 has no requirements for the coating of uncleaned assemblies as it is not even mentioned that it is an option to not clean the assemblies.

Quality requirements in J-STD 001 for conformal coatings include:

- **Thickness**. Acceptable coating thicknesses are specified for five different types of coating materials: Acrylic (0.03-0.13 mm), epoxy (0.03-0.13 mm), urethane (0.03-0.13 mm), silicone (0.05-0.21 mm), paraxylylene[5] (0.01-0.05 mm). The thickness shall be measured on a flat, unencumbered, cured surface of the PCB or a coupon.

- **Uniformity**. Coating distribution and uniformity will depend partly on the method of application and may affect visual appearance and corner coverage. This is expected and is acceptable.

- **Bubbles and voids**. Cured coating should be free of bubbles and voids. However, they are acceptable if they do not bridge noncommon leads or connectors, or expose any conductor. If they do not meet these requirements, they shall be considered as process indicators.

- **Delamination**. The cured coating should be free of blisters and delaminations. As for bubbles and voids, they are acceptable if they do not bridge noncommon leads or connectors, or expose any conductor.

- **Foreign objects debris** (either conductive or nonconductive) in the cured coating shall not bridge conductive surfaces or violate minimum electrical clearance between components, lands or conductive surfaces.

- **Other visual conditions**. The coating shall be free of mealing, cracks, or fisheyes that bridge noncommon conductors and it shall be free of dewetting that exposes a conductor.

It is pointed out in the standard that since the coating thickness is a result of the coating process and is expected to vary on and around components, the coating thickness requirements may not be met at such locations. In fact, due to capillary forces, coating material applied around components may be sucked in underneath the components leaving very little coating material around the components. For leaded components such as QFP components, this means that the solder joints and the component leads may have only a very thin coating which, due to gravitational forces and surface tension, may be extremely thin on the toes and edges of the leads. Due to gravitational forces and surface tension, the coating may also be very thin on top of protruding parts, for example the terminations on ceramic capacitors and ceramic resistors. Consequently, the environmental protection may be poor on leads and terminations to some components, defeating the purpose of applying the conformal coating.

IPC J-STD-001 does not have any requirements that the environmental protection of coated assemblies shall be tested and verified. It is not even discussed how that could be done.

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[5] This is the chemical composition of the coating which is more known as parylene.

# 7. Reliability testing at equipment level

**As discussed in the previous sections, meeting all quality requirements in IPC's standards for manufacturing of soldered assemblies may not be sufficient to assure their reliability.** Therefore, it is common in some industries to require testing at equipment level. For example, in the automotive industry, the end electronic product is usually qualified per the ISO 16750 set of standards [36], although often with modifications of the tests and requirements. In the introduction in Part 1 of this standard, it is stated that *"The user of ISO 16750 is cautioned to understand that the scope of ISO 16750 is limited to conditions and testing at the equipment level, and therefore does not represent all conditions and testing necessary for complete verify- cation and validation of the vehicle system. Environmental and reliability testing of equipment parts and vehicle systems may be required. For example, ISO 16750 does not necessarily ensure that environmental and reliability requirements for solder joints, solderless connections, integrated circuits, and so on are met. Such items are assured at the part, material or assembly level."* In Part 4, it is especially stressed in a note to the temperature cycling test that it is not intended to be a life test.

Since the standards based on "best practice" used during design and manufacture of electronic hardware do not have any reliability requirements, no reliability testing is normally performed at the part, material or assembly level. Still, these are the levels where most reliability issues will show up.

Nevertheless, testing at equipment level may be useful for finding some reliability issues. It can be used to detect design weaknesses and manufacturing defects not detected during manufacturing. An example of a design weakness that can be detected is a design with an inappropriate eigenfrequency and examples of manufacturing defects are "cold solder joints" and "head-in-pillow" defects.

# 8. Physics-of-failure based reliability assurance

## 8.1 Standards for reliability programs

**In the beginning of the 1990s,** the military authorities in U.S. concluded that the traditional practice for assuring reliability of electronic products did not deliver what it was supposed to deliver, reliable and state-of-the-art products. It was realised that it is not possible to require that the products shall be reliable and state-of-the-art while at the same time require that they shall be produced according to standards that in detail regulate how the production shall be performed. Inevitably, situations will occur where these requirements are in conflict with each other and, therefore, one of the requirements has to take precedence over the other. Traditionally, it has been the requirements in standards.

The Headquarters of the Army Material Command (AMC) authorised the Electronic Physics-of-Failure Project to facilitate a more scientific, physics-based approach to electronic equipment reliability in 1992 [37]. In 1994, the Department of Defence (DoD) in US decided to require that a performance-based approach should be used instead of the standards-based approach [38]. When developing a new approach, it is very important that it is well thought-through and that the roles and responsibilities of all partners involved in the developing and manufacturing processes are clearly defined. Therefore, the IEEE Reliability Society was asked to develop a performance-based standard with requirements for a reliability program during product development. As a result, IEEE P1332, Standard Reliability Program for the Development and Production of Electronic Systems and Equipment was published in 1998 [17]. Simultaneously and in co-operation with IEEE, SAE developed a similar standard (SAE JA1000, Reliability Program Standard [18]).

Both the IEEE and SAE standards specify the objectives and the products of required tasks and provide a performance-based framework for determination, achievement and validation of reliability requirements. They are written from the viewpoint of a supplier and provide guidance for how he shall produce products that satisfy the customer (buyer). This is expressed in the form of three objectives (although with slightly differing wording in the two standards).

The supplier shall:

1. Assure that he has understood the requirements of the customer.
2. Develop a process that will satisfy the requirements.
3. Adequately verify that the requirements have been met.

To fulfil these objectives, suppliers and customers are encouraged to co-operatively integrate their reliability processes and have a dialogue which establishes required product characteristics, ensures that product use is fully understood, and determines quantifiable supplier-understood requirements. The supplier shall receive from the customer all available important

usage and environmental condition information, such as how the product will be used, by whom and where, and expected lifetime specifications. Neither the standard nor the customer specifies the tasks to be performed. The supplier is free to use innovative means to develop the product. Every product demands a reliability program specifically structured to its circumstances. Therefore, the supplier shall tailor a reliability program based on customer requirements, product needs, and the methods chosen to meet them. In an implementation guide to the SAE standard [39], this new approach is described as a transition from a "*fixed document approach*" to a "*performance based, supplier-customer dialogue approach*".

To be able to do that, the supplier must understand how the reliability may be affected by the design and manufacturing processes. He is then responsible for choosing test methods for adequately verifying that reliability requirements are met. In the implementation guide to the SAE standard [39], it is stressed that: *Reliability efforts must be directed toward anticipating problems and designing-in features that assure the achievement of quality and reliability, concurrent with the development process, instead of trying to assess quality and reliability downstream.* This requires knowledge of the failure mechanisms that may be critical for the reliability and the physics-of-failure for these failure mechanisms. Hence, this approach is often called a "physics-of-failure", "knowledge-based" or "performance based" approach.

In 2007, it was again concluded that a significant number of U.S. Army systems had reliability problems [40]. In a memorandum from 2011, it was estimated that approximately four out of five U.S. Army systems fail to achieve their reliability requirements [41]. To improve the reliability, the US DoD supported the development of a new reliability standard [42]. This standard was published as ANSI/GEIA-STD-0009, Reliability Program Standard for Systems Design, Development, and Manufacturing in 2008 [43]. A Reliability Program Handbook (TA-HB-0009) was also published in 2013 [44].

The GEIA standard is based on the IEEE and SAE standards for reliability program and has the same performance-based approach. However, whereas the IEEE and SAE standards are very general and consist only of a few pages each, the GEIA standard is much more specific in describing necessary activities to achieve reliable products. The focus is not only on designing reliable products, but also on assuring reliability of production processes and on monitoring and managing reliability during the development and use of the products.

In the foreword to the GEIA standard, it is stated that it "*describes the kinds of reliability management practices and reliability design and testing activities the customer will want developers to propose. A reliability standard is needed that aligns with best practices, but is not prescriptive in terms of reliability tasks or methods to be performed. Rather, developers are considered equal partners in deciding which reliability methods are applicable. This standard addresses those needs.*

*This standard is intended to align best practices of reliability management, design and testing with reliability methods that provide the most value and the least risk in terms of achieving reliable products. The demand for highly-reliable systems/products prompted the development of a new standard that specifies a* ***scientific approach*** *to reliability design, assessment, and verification, coupled with integrated management and systems engineering. This standard defines "what to do" in order to* ***design and build reliability in****, then maintain high reliability when the system/product is in the hands of the user."*

It is also pointed out in the standard that "*a successful reliability program is greatly dependent on the demonstrated level of commitment by user's, customer's, and developer's program management, particularly at the upper levels. This commitment can be reinforced by ensuring that the reliability program is an integral part of the business strategy with an optimum funding profile for design, development, verification and demonstration, and operation.*"

To achieve reliable products, the GEIA standard requires that:

- Developers/contractors and customers/users work as a team through the whole product development process to plan and implement a reliability program that provides systems/products that satisfy the user's requirements and expectations over their life cycle.

- The developer, working with the customer and user, shall include the activities necessary to ensure that the user's requirements and product needs are fully understood and defined, so that a comprehensive design specification and Reliability Program Plan can be generated.

- The developer shall use well-defined reliability- and systems-engineering processes to develop, design, and verify that the system/product meets the user's documented reliability requirements and needs.

- Multifunctional groups consisting of individuals representing various product disciplines such as engineering, manufacturing, software, quality, reliability, etc. shall collaborate during each phase of the program and verify during production that the developer has met the user's reliability requirements and needs prior to fielding.

- The multifunctional team shall monitor and assess the reliability of the system/product in the field.

The methodology used in the standard can be summarised in three points [45]:

1. Progressive understanding of the system-level operational and environmental loads and the resulting loads and stresses that occur throughout the structure of the system.

2. Progressive identification of the resulting failure modes and mechanisms.

3. Aggressive mitigation of surfaced failure modes.

That is, the focus is on ***risk management***, i.e. the identification and minimisation of the risks for reliability problems, both regarding the product and production processes. In order to not cause delays in product development, the work should be focused on proactively qualifying the materials, design and manufacturing processes used to produce the product rather than the end product itself. To save time and money, modelling & simulation may be a useful tool to use alone or in combination with testing to verify reliability.

A new revised version of the standard, GEIA-STD-0009A, was released in 2020 by SAE.

See references 1, 46 and 47 for a more extended discussion of this topic and more detailed descriptions of the of the standards for reliability programs.

## 8.2 Assuring reliability according to reliability program standards

**The activities required in the reliability program standards have as goal** not only to assure reliability but also to facilitate the release of a new product in as short time as possible. Basically, the activities are in line with the activities in concurrent engineering that was developed in the 1990s [48], but with the main focus on reliability issues and, perhaps, a stronger involvement of the customer/user in the development process.

Concurrent engineering has been defined as [25]:

*"A systematic approach to the integrated, concurrent design of products and their related processes, including manufacture, and support. This approach is intended to cause the developers, from the outset, to consider all elements of the product life cycle from concept through disposal including quality, cost, schedule, and user requirements."*

That is, a design team needs to be formed that cover all appropriate issues of design, packaging, manufacturability, testability, reliability, maintainability, environmental compatibility, etc. According to Blackwell [25]:

*"This is more than the customary committee. Although the team is composed of specialists from the various activities, the team members are not there as representatives of their organisational home. They are there to cooperate in the delivery of product to the market place by contributing their expertise in the task of eliminating the redesign loops."*

If concurrent engineering shall be successfully implemented, it is important to realise that implementing concurrent engineering is more than a process change, or as expressed by Blackwell [25]:

*"Concurrent engineering is as much a cultural change as it is a process change. For this reason it is usually achieved with some trauma. The extent of the trauma is dependent on the willingness of people to accept change, which in turn is dependent on the commitment and sales skills of those responsible for installing the concurrent engineering culture. Although it is not usually necessary to re-engineer, that is, to restructure, an entire organisation to install concurrent engineering, it is also true that it cannot be installed like an overlay on top of most existing structures. Although some structural changes may be necessary, the most important change is in attitude, in culture. Yet it must also be emphasized that there is no one size fits all pattern. Each organisation must study itself to determine how best to install concurrent engineering."* Also *"The importance of commitment to a concurrent engineering culture from top management to line workers cannot be emphasized too strongly."*

Accordingly, the need for cultural changes in assurance of product reliability was stressed in Perry's memorandum on the Military Specifications and Standards Reform [38].

Obviously, meeting the requirements in the reliability program standards is a huge task, especially for the GEIA standard. Only very large companies will have the resources required for that. Nevertheless, I believe most companies would benefit from adopting a more performance-based approach for assuring reliability based on the reliability program standards. How this should be done will depend on the circumstances for each company and the resources they have. However, the focus should be on risk management, i.e. identification and minimisation of risks for reliability problems. This should be an integral part during the whole product development process. Preferably, all participants in the supply chain should be involved in assuring reliability, but that is often difficult to achieve due to extensive outsourcing.

# 9. Failure mechanisms at assembly level

**The physics-of-failure approach in the IEEE, SAE and GEIA standards for reliability program requires knowledge of the failure mechanisms that may be critical for the reliability, the physics-of-failure for these failure mechanisms, but also how to adequately verify that reliability requirements have been met.**

This part of the document describes common failure mechanisms for soldered assemblies and test methods for evaluating how they affect reliability at assembly level. The focus is on failures of defect-free assemblies. That is, failures due to manufacturing defects are not covered.

## 9.1 Common causes of failures for soldered assemblies

**The main causes for failures of soldered** printed board assemblies at PCB and assembly level are:

- Failures of solder joints.
- Electrochemical migration.
- Interconnect failures in PCBs.

Various factors affecting these types of failures will be described in the following sections with the main focus on the two first causes for failures.

## 9.2 Formation of solder joints

**To understand the physics-of-failure for solder joints**, it is important to understand the reactions that occur when solder joints are formed and how these reactions are affected by the composition of the solder and the surfaces that the solder joints are formed to. The reactions that occur with tin-lead solder will be compared with reactions that occur with lead-free solders based on tin with additions of silver and copper (SAC solders).

Tin-lead solders consist of two phases, one tin-rich with a very low content of dissolved lead and one lead-rich phase with a very low content of dissolved tin. A typical appearance of a eutectic SnPb solder (63 % Sn and 37 % Pb) is shown in Figure 1.

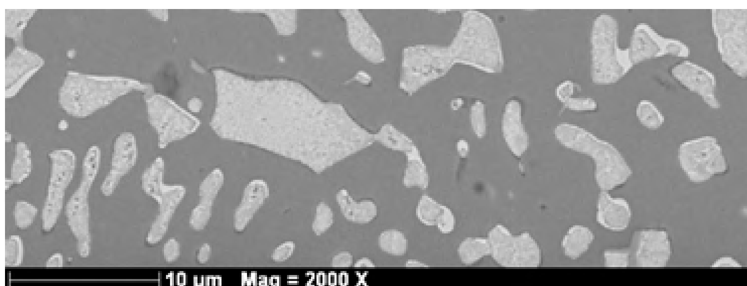


*Figure 1 Appearance of eutectic Sn-Pb solder with lead grains (light grey) embedded in a matrix with the tin phase (dark grey).*

The morphology of SAC solders is quite different. The main reason is that silver and copper, which have very low solubility in tin, form intermetallic compounds (IMCs) with tin, $Ag_3Sn$ and $Cu_6Sn_5$, respectively. Lead does not form intermetallic compounds with tin.

Another reason is that SAC solders require an undercooling of typically 15-80 °C before they solidify [49, 50, 51]. The degree of undercooling depends on many factors including solder composition, solder volume, cooling rate and surface finishes on soldered surfaces. Small solder volume [49, 52] and high cooling rate increase the degree of undercooling. Before solidification can occur, a tin nucleus needs to be formed. This is normally formed on a surface to which soldering is done, usually on the PCB side [53, 54]. Once a tin nucleus has formed, the solidification occurs very quickly. It may take only fractions of a second for complete solidification [54, 55]. Therefore, solidification usually starts from only one nucleus, but it may start from more than one nucleus. According to Lee.et al., it may occur about 1 % of the time [56], but there are only a few reports in the literature of solder joints showing more than one nucleation site [5, 49, 57, 58, 59]. The image to the left in Figure 6 shows a solder joint where solidification has started from at least two nuclei.

Due to the low solubility of silver and copper in tin, primary tin dendrite arms are first formed consisting of almost pure tin when the solder solidify in a solder joint [60]. The Ag and Cu in the solder will be enriched in regions with still melted tin surrounding the tin dendritic arms. When these regions solidify, ternary eutectic interdendritic regions are formed consisting of a tin matrix with inclusions of a large number of small (secondary) precipitated particles of $Ag_3Sn$ and $Cu_6Sn_5$ IMCs [54, 60, 61]. Figure *2* 2 shows a cross-section of a solder joint with dendrite arms surrounded by interdendritic regions with inclusions of small IMCs.

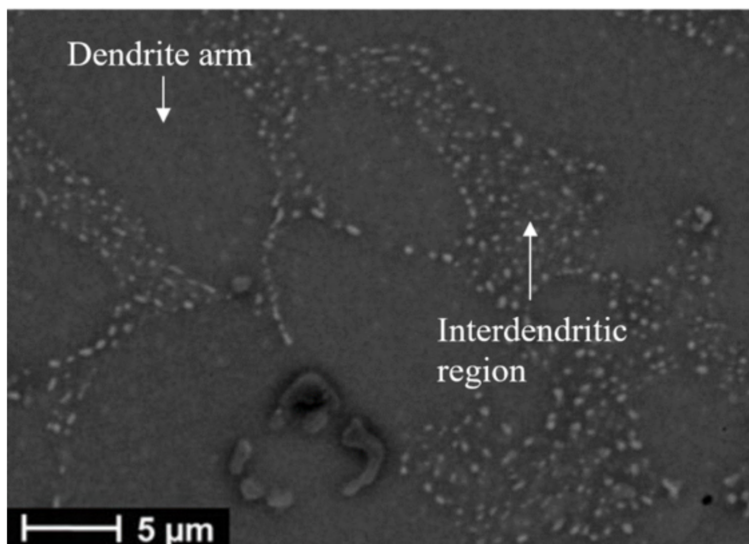


*Figure 2 - Microstructure of solder joint showing dendrite arms and interdendritic regions [62].*

When a solder joint is formed, metal from the surface to be soldered dissolves in the melted solder (a prerequisite for forming a good solder joint). After a short time, the melted solder will be oversaturated with the dissolved metal and a layer with an intermetallic compound consisting of tin and the dissolved metal will be precipitated on the metal surface. Although many different types of surface finishes are used on component leads and terminations, and solder pads, the IMC layers are almost exclusively formed to one of three metal surfaces: copper,

electrolytic nickel, or electroless nickel. Other thin finishes plated on top of these, such as silver, gold and palladium, are normally completely dissolved in the solder.

The thickness and composition of the IMC layer formed for various combinations of solders and surface finishes are affected by many factors.

When the solder joint is formed to copper, the IMC layer will normally consist of $Cu_6Sn_5$ (Figure 3a and c). These crystals, which usually have a scallop-like appearance, will grow and after a soldering process they will completely cover the surface. The IMC layer formed has an uneven thickness, normally in the range 0.5 to 2 µm. The IMC layer will be the same both when soldering with SnPb and lead-free solders, but it may be a little thicker when soldering with SAC solders due to the content of Cu in the solder.

It is more complicated when the solder joint is formed to nickel. If the solder does not contain copper, i.e. SnPb and SnAg solders, the IMC layer will consist of $Ni_3Sn_4$. When soldering to nickel surfaces using lead-free solders containing copper, the copper content in the solder will be important for the composition and structure of the IMC layer(s) formed. If the solder contains more than 0.6% Cu, $Cu_6Sn_5$ will form but with some of the copper atoms exchanged against nickel atoms. That is, the composition will be $(Cu,Ni)_6Sn_5$ (Figure 3b). At copper concentrations below 0.4 %, a dual IMC layer may form consisting of $(Cu,Ni)_6Sn_5$ and $(Ni,Cu)_3Sn_4$. The latter phase is the same as $Ni_3Sn_4$, but with some of the nickel atoms exchanged with copper atoms and is formed closest to the nickel surface. This dual layer may also form when solder joints with more than 0.6% Cu are aged.

If the solder joint is formed between a copper surface and a nickel surface, copper-containing IMC layers may also form on the nickel surface even when soldering using a copper free solder due to copper dissolved form the copper surface. Similarly, nickel dissolved from the nickel surface may affect the IMC layer formed on the copper surface by replacing some of the copper atoms with nickel atoms, i.e. $(Cu,Ni)_6Sn_5$ will form also in this case (Figure 3d). The IMC layer may then become 2-3 times thicker compared to when no nickel is present.

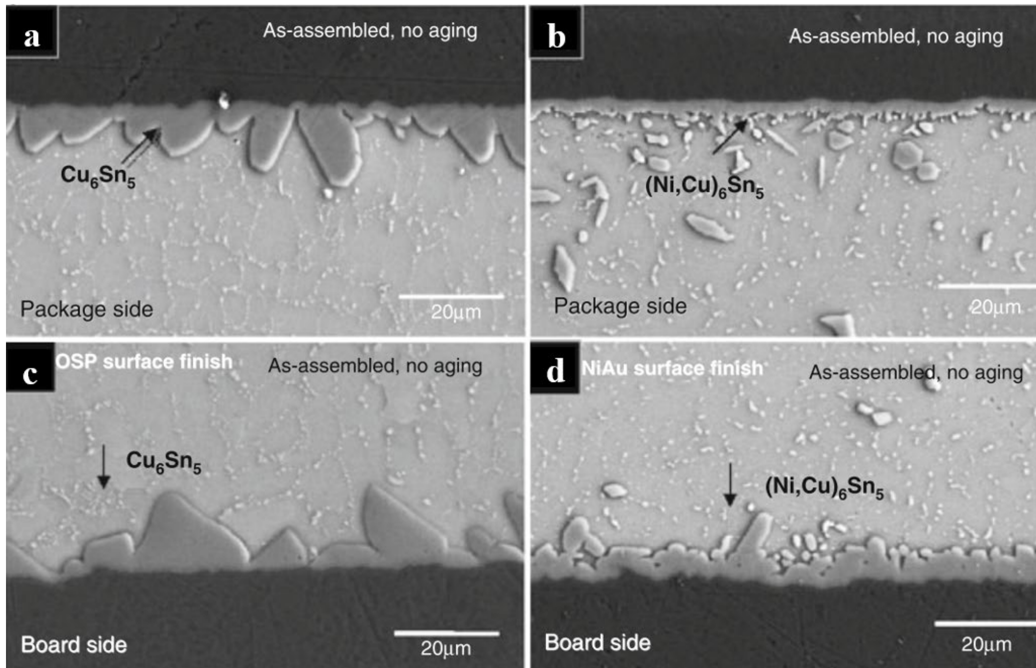


*Figure 3 - Solder joints to BGA components with SAC solder balls soldered to a PCB with copper pads. In images a and c, the solder joints are formed to copper (OSP) pads on the BGA whereas they in images b and d are formed to electrolytic NiAu [63].*

When solder joints to copper with an IMC layer consisting of $Cu_6Sn_5$ are exposed to high temperatures, a second IMC layer consisting of $Cu_3Sn$ will form at the $Cu_6Sn_5$/Cu interface, i.e. a double IMC layer is formed. This reaction will be faster the higher the temperature. In some cases, extensive formation of Kirkendall voids may occur in the $Cu_3Sn$ layer or at the $Cu_3Sn$/Cu interface when exposed to temperatures above 100 °C, perhaps even at lower temperatures [64, 65]. The formation of Kirkendall voids results in a significantly increased risk for fractures in the IMC layer. Impurities in the copper and the higher soldering temperature used for lead-free soldering seem to be the main causes for the formation of Kirkendall voids.

A more detailed description of the composition and thickness of IMC layers formed with various combinations of solders and surface finishes and how they affect the risk for fractures in the IMC layers are given in references 2 and 66.

## 9.3 Grain structures in lead-free solder joints

**Lead-free solder joints based** on tin, silver and copper usually have one of four common grain structures. When solidification occurs at not too large undercooling, the whole solder joint may consist of one single tin grain with embedded IMC particles, i.e. a single-grained (SG) structure.

Another possible structure is cyclic twin (CT) structure. In cross-sections of solder joints to BGA components with cyclic twins, they sometimes have an appearance of a beach ball consisting of seemingly six grains. However, only three unique grain orientations are present which nominally have an about 60 degrees rotations around a common axis. In both SG and CT structures, each grain consists of a parallel array of Sn dendrites that have grown from one solidification nucleus.

When cross-sections are analysed using either polarised light or electron backscatter diffraction (EBSD), grains with different orientation will have different colours. Figure 4 shows a solder joint to a BGA component with a slightly distorted beach ball structure analysed using these methods. Though, more typically, the grains in solder joints with cycling twin structure are fewer, more irregular and do not have an appearance of a beach ball in a cross-section [57].

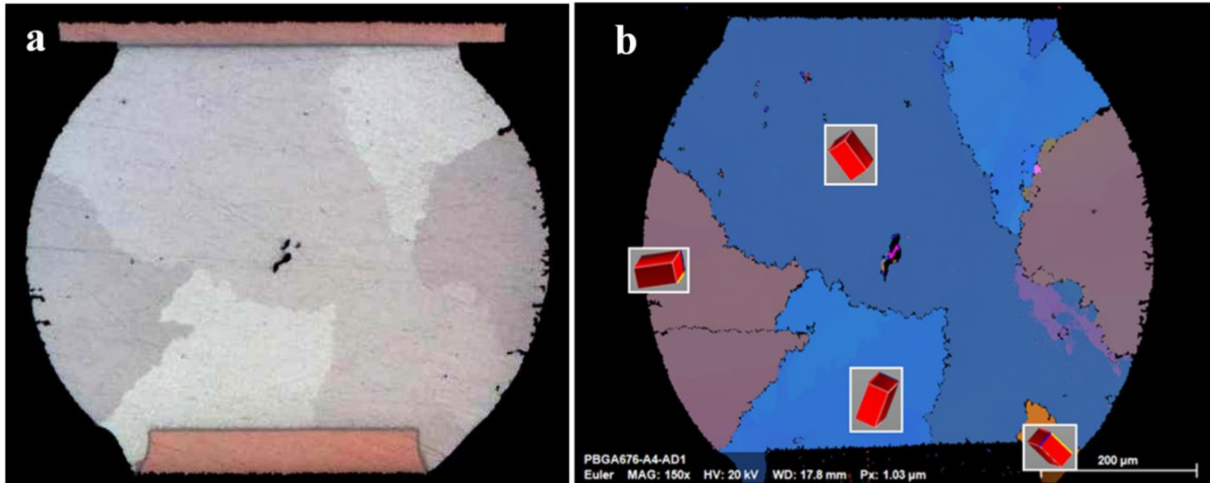


*Figure 4 - SAC solder joint to a BGA676 component examined using (a) polarised light and (b) electron backscatter diffraction showing a cyclic twin structure. Grains with the same orientation have the same colour.*

At high degrees of undercooling, solder joints may instead get an interlaced twin (IT) structure. Although this structure seems to have the appearance of a finegrained polycrystalline structure, as shown in Figure 5, it is not a polycrystalline structure. As for the CT structure, only three unique grain orientations are present with about 60 degrees rotations about a common axis.

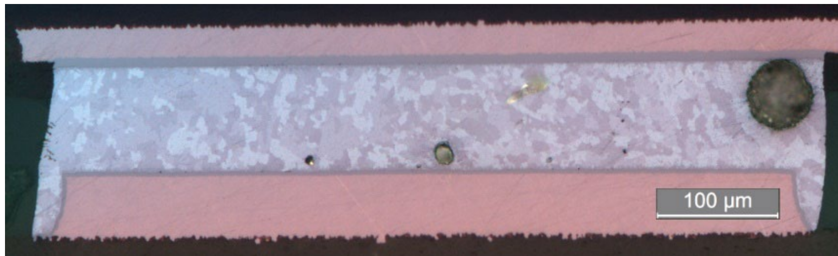


*Figure 5 - SAC solder joint to a land grid array (LGA) component examined using polarised light showing interlaced twin structure.*

Sometimes the first part of the solder joint that solidify may have an interlaced twin structure whereas the rest of the solder joint has a cyclic twin structure. Solder joints with such mixed CT/IT structure are shown in Figure 6. Normally, the part that has an IT structure is formed at one of the two solder pads.

The solidification is an exothermic reaction. That is, the solder is heated during solidification, sometimes up to the melting temperature of the solder. That may explain why the solidifycation changes from IT structure to CT structure.

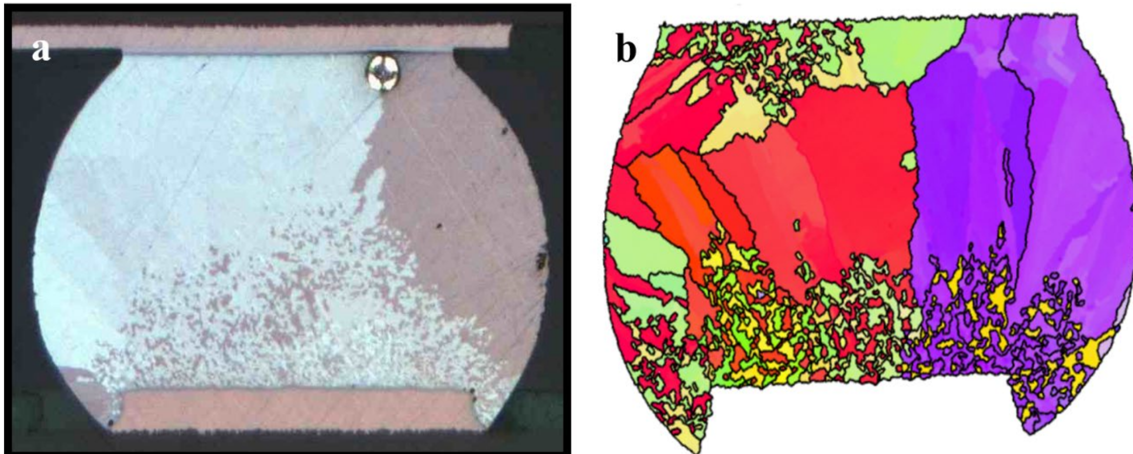


*Figure 6 - Solder joints to BGA components with mixed cyclic and interlaced twin structures examined using a) polarised light and b) EBSD [5].*

See references 5, 7 and 67 for a more extended discussion of how various factors affect the grain structure in solder joints and the impact of grain structure on solder joint fatigue.

## 9.4 Failure mechanisms of solder joints to components

**Besides failures due to poor quality of solder joints** (which will not be covered in this document), there are two main failure mechanisms for solder joints, fatigue fractures and brittle fractures.

Since components and PCBs usually have differing coefficients of thermal expansion (CTE), a change in temperature will cause thermo-mechanical stress on the solder joints due to this global expansion mismatch. Local CTE mismatch between the solder and soldered surfaces may also cause local thermo-mechanical stress on the solder joints close to the soldered surfaces, especially for ceramic components [68]. Thermo-mechanical stress may also be caused by heat generated in components (power dissipation) when the product is used resulting in temperature gradients between the components and the PCB.

When a solder is exposed to stress, it will start to deform. At low stress levels, the deformation is elastic (reversible) but above the yield stress it becomes plastic (irreversible). If a material is exposed to a constant stress above the yield stress, an ongoing plastic deformation will occur as long as the load is applied. This deformation is called creep. The larger the load is, the faster the creep. The creep rate also depends on how close the material is to its melting temperature, which is expressed as its homologues temperature (the temperature of the material divided by

its melting temperature in Kelvin). For materials with a homologues temperature above about 0.5, creep will occur even at very low stress levels. Since tin-lead solders and lead-free solders based on tin, silver and copper have homologues temperatures of about -45 °C and -25 °C, respectively, creep will occur in most conditions that electronic products are used.

Fatigue results when a cyclic stress or cyclic strain is applied to the material [69]. It is usually split into two fatigue regimes based on the number of cycles-to-failure ($N_f$). Low-cycle fatigue (LCF) is characterised by $N_f$ <10.000 cycles and high-cycle fatigue (HCF) by $N_f$ >10.000 cycles.

For materials prone to creep, such as solder, the applied stress has a minor influence on the number of cycles to failure. Instead, the time the solder is allowed to creep in each cycle is the factor that has the largest impact on $N_f$. Therefore, low-cycle fatigue is usually associated with thermal cycling loads since the time solder is given to creep during thermal cycling usually is long. Accordingly, high-cycle fatigue is typically associated with mechanical or vibration cyclic loads since the time solder joints are allowed to creep then is very short. Only LCF will be covered in this document.

When creep occurs in solder joints exposed to temperature cycles, i.e. LCF, the resulting deformation will first cause formation of microvoids. When the cyclic stress continues, new microvoids will form with every cycle and coalesce to large defects. The larger the deformation per cycle, the larger the microvoids formed. With time, these will develop to a ductile fatigue fracture in the solder joint.

If solder joints are exposed to high strain and/or high strain rates, it may result in another type of fracture that occurs in the IMC layers formed at the interfaces between the solder and soldered surfaces. These fractures have a brittle appearance. Components having no leads, such as BGA components, are especially vulnerable to this type of fracturing since leads will take up much of the stress. A complete crack may be the result of one single event or several sequential events (Figure 7). Typical incidents that can cause brittle fracture are fast temperature changes, dropping a product on the floor, bending of an assembly and high vibration levels.

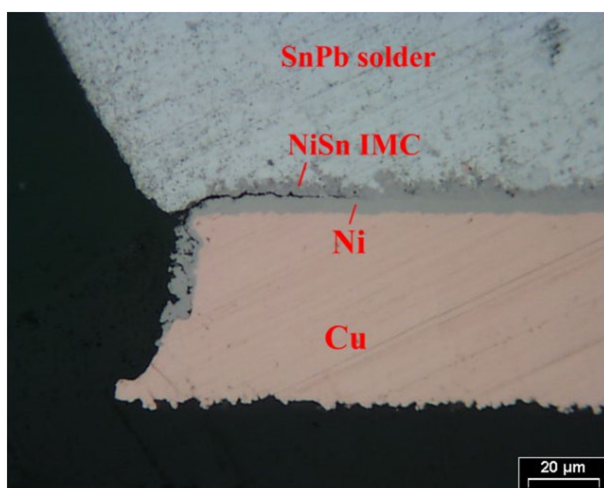


*Figure 7 - Cross-section of a solder joint to a BGA component showing an initiated brittle crack formed in a nickel-tin IMC layer at the interface between tin-lead solder and a nickel layer on the solder pad.*

Stress on solder joints may also cause fractures in the PCB laminate and in components. Figure 8 illustrates the types of cracks and where they can occur for BGA components. They may occur on either the PCB or component side of a solder joint. Fractures that occur in the PCB laminate may cause pad lift. This latter type of cracking is usually called "pad cratering" since it leaves a crater in the PCB/component (see section 9.8.2).

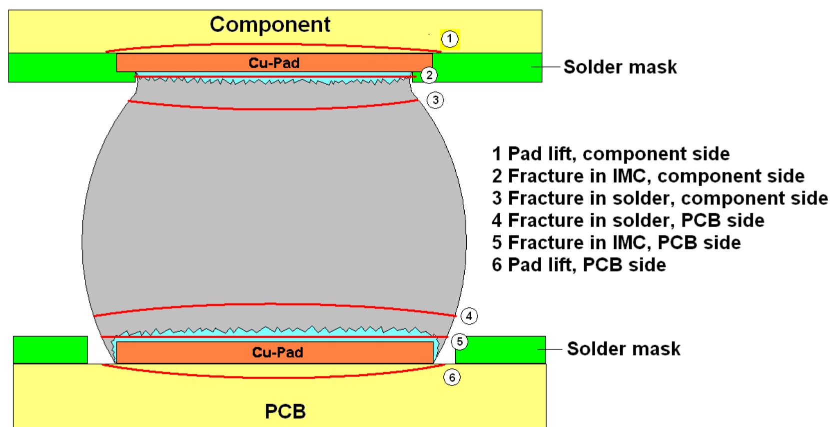


*Figure 8 - Different types of fracture sites for a solder joint to a BGA component.*

# 9.5 Factors affecting fatigue fractures in solder joints

## 9.5.1 Solder joints to ball grid array components

Ball grid array (BGA) components consist of a large group of components that may have very different build-up and properties. The common factor is that the bottom side of the components have an array of solder balls, and the solder joints are formed directly to solder pads on the PCB. That is, the connections between the components and the PCB consist only of solder.

The fatigue life of solder joints to BGA components will be affected by anything that might affect the stress levels on the solder joints. This can be caused by a large number of factors of which the most important are:

- Build-up of the component. (10)
- Flip chip mounted chip or wire bonded. (2)
- Dimensions of the component. (10)
- Dimensions of internal chip(s). (10)
- Die attach material: Thickness and elasticity. (5)
- Component substrate: Thickness, CTE, elasticity and brittleness. (10)
- Moulding compound: Glass transition temperature ($T_g$), CTE and elasticity. (5)

- Location of solder balls: Full array or reduced array, underneath the chip or not underneath the chip. (10)
- Pitch. (8)
- Solder balls: Size and composition. (20)
- PCB: Build-up, thickness, CTE and $T_g$. (20)
- Solder pad definition. (2)
- Surface finish on solder pads. (7)
- Soldering profile. (3)
- Applied conformal coating.
- Applied underfill.

If you will not apply a conformal coating or an underfill and assume that the various factors can have the number of levels given in parentheses (which is a bit low for most of them), the number of possible combinations of major factors that affect reliability of solder joints to BGA components will be 672 billion. That is more than the number of stars in our galaxy, the Milky Way, which is estimated to be 100-400 billion. That gives an indication of how difficult it is to forecast the reliability of a certain combination of these factors without testing. Further-more, if you read a paper presenting results from an evaluation of the fatigue life of solder joints to BGA components, normally only a few of these factors are specified. Therefore, caution should be exercised when comparing results from various evaluations. Factors not specified, but important for the fatigue of the solder joints, may be different in the evaluations.

In the following sections, it will be described how most of these factors may affect the fatigue of solder joints to area array components.

## Build-up of BGA components

Some of the more common BGA types are described below.

**Plastic ball grid array components**

One of the most common types of BGA components used is the plastic BGA component of OMPAC type (overmolded plastic pad array carrier). The main characteristics of these plastic BGAs are illustrated in Figure 9, although are wide variations.***Fel! Hittar inte referenskälla.***

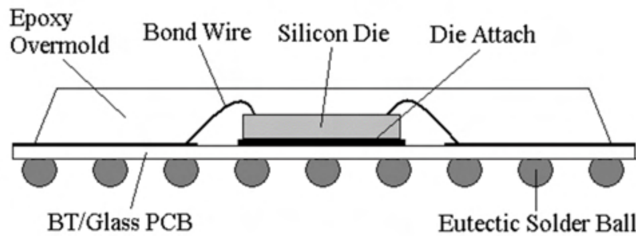


*Figure 9 - Schematic cross-section of a plastic BGA of OMPAC type.*

A double-sided or multilayer organic substrate is the base in the package. Bismaleimide-triazine (BT) is the most common substrate, but FR-4 and flex films are also used. The chip is usually attached to the substrate using a die attach adhesive. The chip is then wire-bonded to the substrate. The wire bonds and the chip are protected by an epoxy overmould. Alternatively, flip-chip technology may be used to connect the chip to the substrate. On the bottom side of the substrate, solder balls are reflow-soldered to solder pads. Near eutectic solder balls are mostly used, but solder balls made of high temperature melting solder is also used. Usually, the surface finish of the solder pads is either electrolytic nickel/gold, electroless nickel/immersion gold (ENIG) or organic solderability preservative (OSP).

**Super ball grid array components**

An alternative build-up of a BGA is to mount the chip on a metal carrier with the chip turned down. There are numerous types of BGA versions constructed using this technology. One of the first developed is a package called SuperBGA (SBGA) developed by Amkor/Anam (Figure 10). In this package, the chip is wire-bonded to a thin BT substrate with 1 or 2 metal layers [70]. The BT substrate is attached to a heat-coupling copper ring. Both the copper ring and the chip are attached to a copper heat sink. It has been shown to have approximately 4 times better fatigue life than BGA components of OMPAC type with about the same number of balls and chip size due to better CTE match to an organic PCB [70]. However, due to the built-up, the package is only available with perimeter array and therefore needs to be considerably larger than the chip.

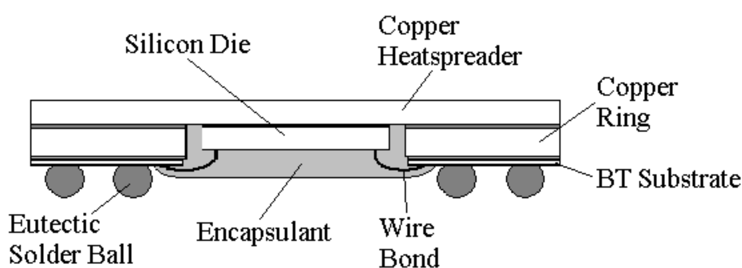


*Figure 10 - Schematic cross-section of an SBGA*

**Ceramic ball grid array components**

For space and military applications, ceramic BGAs (CBGAs) are common. The schematic build-up of ceramic packages is shown in Figure 11 [71]. Ceramic BGA packages use cofired multilayer or pressed ceramic substrates. The chip can be protected using a variety of lid sealing or encapsulation techniques. To increase the stand-off of the components, and thereby improve the fatigue life of the solder joints, non-melting solder balls are used. These usually consist of tin-lead solder with 90 % lead and a melting temperature of 302 °C. Nevertheless, because of the large CTE difference between a ceramic package and an organic PCB, the fatigue life of the solder joints will be relatively short. A method to improve the fatigue life of the solder connections is to replace the solder balls with columns of high temperature melting tin-lead solder or copper with a height of 1.27 mm to 2.2 mm. Both balls and columns are usually attached to the package using eutectic tin-lead solder.

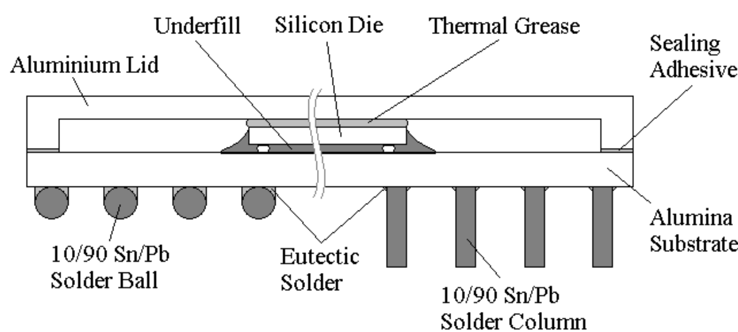


*Figure 11 - Schematic cross-section of a ceramic solder-grid-array with solder balls or columns.*

More examples of BGA types can be found in the very extensive guideline for design and assembly process implementation for BGAs in the IPC standard IPC-7095 [34]. As the title implies, it also contains guidelines for design and manufacturing of assemblies with BGA components.

**Wafer level packages**

Wafer level packages (WLPs) belong to the group of BGA components. They can be divided into two groups. Fan-in wafer-level packaging is a technology of packaging the chip while it is still on the wafer. Protective layers and electrical connections are added to the substrate before dicing. That is, the resulting package is practically of the same size as the chip. The protective layers between the chip and the solder pads are very thin. Common pitches for WLP components are 0.3 to 0.5 mm. Due to the thin protective layers between the chip and the solder pads, the components will in principle have the same CTE as the chip, i.e. about 3 ppm/°C. Since an organic PCB normally have a CTE of about 16 ppm/°C in the plane parallel to the PCB surface, there is a very large CTE mismatch between WLP components and a PCB. This together with the small pitches lead to very short fatigue life of solder joints. Except for very small WLP components, solder joints to these components may have fatigue lives that are only a few percent of the fatigue lives of solder joints to QFP components.

Another group of WLPs is fan-out WLPs. In fan-out wafer level packaging, the wafer is diced first. Then the chips are very precisely re-positioned on a carrier wafer or panel, with space for fan-out kept around each chip. The carrier is then reconstituted by moulding, followed by making a redistribution layer atop the entire moulded area (both on the chip and the adjacent fan-out area), and then forming solder balls on top. It allows placing more solder balls on the

bottom side of the component but, as long as some solder balls are located underneath the chip, it will not improve the fatigue life of the solder joints underneath the chip.

A thorough guideline for design and assembly process implementation for WLPs can be found in the IPC standard IPC-7094 [33].

### Chip size, substrate thickness and perimeter arrays

Ceramic BGAs and WLP components are very stiff components and the CTEs of the components are almost entirely determined by the ceramic material and the chip, respectively.

The CTE of packages of OMPAC type, on the other, is affected by many factors. Since the silicon chip has a very low CTE and is very stiff, it will constrain the substrate's CTE in the region of the chip [72]. Thus, solder joints located underneath the edges of the chip will usually experience the highest amount of strain during thermal excursions and will be the first solder joints to fail [72, 73]. Since the stress on the solder joints will be higher the larger the size of the chip, the fatigue life will decrease with increasing size of the chip [72, 74]. An increase of the thickness of the chip decreases also the fatigue life of the solder joints beneath the chip [72]. A way to improve the fatigue life is to avoid placing solder balls on the surface beneath the chip (perimeter array) [75] but that will increase the size of the component and may impair the electrical properties.

Instead, the reliability of solder joints to packages of OMPAC type can be improved by decreasing the influence of the chip on the substrate's CTE [72, 75, 76, 77, 78]. This can be done by increasing the substrate thickness, decreasing the chip size and thickness, using a thicker die attach or a die attach with lower Young's modules. Figure 12 shows the impact of the thickness of the substrate and the elasticity of the die attach (DA) on the CTE of the BGA substrate as a function of the distance to the neutral point – DNP (centre of the component). This means that two BGAs looking identical from the outside may have very different solder joint fatigue properties.

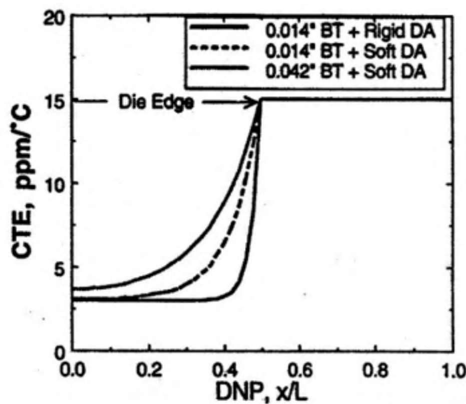


*Figure 12 - Impact of the thickness of the substrate and the elasticity of the die attach (DA) on the CTE of the BGA substrate as a function of the DNP [72].*

## Pitch

In order to improve the functionality of components, there is a continuous strong pressure to decrease their size. This necessitates a decrease of the pitch for BGA components. The BGA components that were first developed in the nineties had pitches of 1.5 mm to 1.27 mm. In the late nineties, BGA components with 1.0 mm, 0.8 mm and 0.75 mm pitch became common [74]. Today, fine pitch BGA components with 0.4 mm to 0.5 mm pitch are common and even smaller pitches occur.

A reduction in pitch for BGA components typically causes a reduction in fatigue life for several reasons. First, for BGAs having a peripheral array, it will bring the solder joints closer to the edge of the chip or they may even be located underneath the chip [74, 79]. Decreased solder pad size and stand-off will also contribute to reduced fatigue life.

## Surface finish on PCB and component pads

A large number of finishes is used on PCBs. The most common are:

- Hot air solder levelled (HASL) with SnPb or lead-free solders
- Electroless nickel/immersion gold (ENIG)
- Organic solderability preservative (OSP)
- Immersion silver
- Immersion tin

The choice of surface finish on the PCB affects soldering processes (for example shelf life and solderability) but it also affects the reliability of solder joints. Since HASL is applied in a soldering process, it is necessary to use flux in this process. The flux used in HASL is usually very highly activated and there will always be some flux residues remaining on the PCB that will affect SIR. Since even more activated fluxes are required for lead-free HASL, it may have larger negative impact on SIR.

The most common finishes used on BGA components are:

- Electrolytic nickel/electrolytic gold
- Electroless nickel/immersion gold (ENIG)
- Organic solderability preservative (OSP)

Since the surface finishes will affect the composition and thickness of the IMC layers formed, the failure mechanism that is most affected by the surface finishes is brittle fracturing in the IMC layers. Solder joints to ENIG is known to be prone to brittle fractures even when the solder joints consist of SnPb solders. As even small changes in the composition of the solder may cause large changes in the thickness and composition of the IMC layer, the combination of solder and surface finish used is very important for the inclination for brittle fractures.

The choice of surface finish on the solder pads may also affect the degree of undercooling before solidification starts. Since that affects the grain structure in the solder joints [5], the combination of surface finishes on the component and PCB pads may also affect the fatigue life of the solder joints.

## Solder pad definition

Two alternative methods for definition of the solderable surface of solder pads on BGAs and PCBs are commonly used: Solder mask defined (SMD) and non-solder mask defined (NSMD) solder pads. For SMD pads, the diameter of the solder mask opening is smaller than the diameter of the solder pad, whereas it is larger for NSMD pads (Figure 13). By using SMD pads, the area of the pad can be increased without increasing the solderable area giving better adhesion of the solder pads to the substrate.

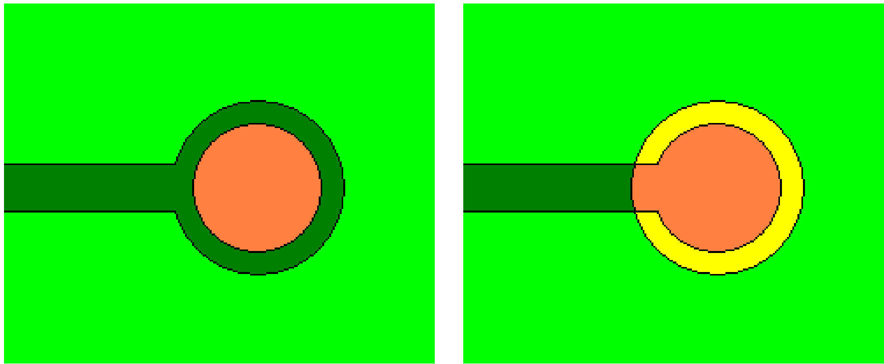

*Figure 13 - Solder mask defined (left) and non-solder mask defined (right) pads with the same solderable area.*

The type of definition of the solderable area affects the geometry of the solder joint as shown in Figure 14. With the same solderable areas and the same solder volume, SMD pads will give some what higher stand-off distance. Nevertheless, reliability testing has shown that SMD pads give inferior fatigue life compared to NSMD pads [80, 81]. The reason can be found in the geometry of the solder joints as shown in Figure 15.  With the same solderable surface, the diameter of the solder joints close to the solder pads will be larger for NSMD pads resulting in less strain during thermal cycling. Furthermore, when SMD pads are used, they introduce stress concentration points where cracks easily can be initiated and grew parallel to the solder pad.

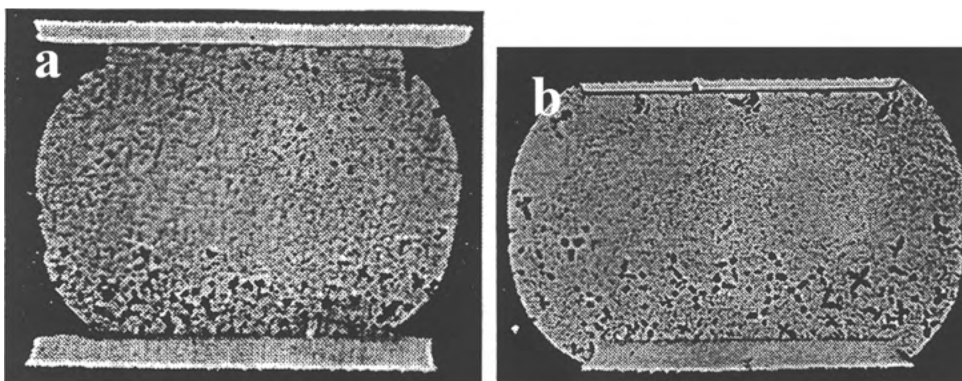


*Figure 14 - Geometry of solder joints formed with a) SMD pads and b) NSMD pads.*

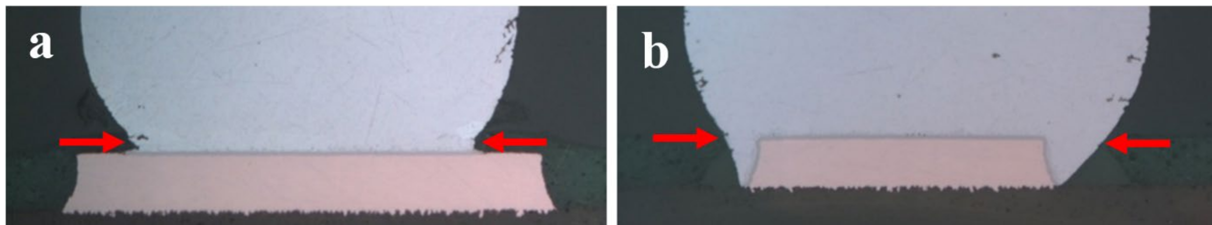


*Figure 15 - The arrows mark the points with highest strain for a) SMD pads and b) NSMD pads.*

NSMD pads have been shown to give approximately twice as long fatigue life as SMD pads [80, 81, 82], but then the pads need to be NSMD on both the PCB and the component. A drawback with NSMD pad is that the copper pad may be ripped off from the component substrate. Since this has been a problem for BGAs, and the copper pad has a much larger diameter for an SMD pad than an NSMD pad (with the same solderable area), SMD pads are often used on BGA components. This is much less an issue on the PCB since the copper pad normally has better adhesion to PCBs.

Using an NSMD pad on the PCB with the same solderable area as an SMD pad on a BGA will lead to an asymmetric solder joint with larger diameter to the PCB side of the solder joint (Figure 16). This will promote more creep on the component side of the solder joint resulting in a shorter fatigue life compared to a more symmetric solder joint. To achieve a more symmetric joint for BGAs having SMD pads but still use NSMD pad on the PCB, the pad diameter for the NSMD pads should be reduced with about 15 % [83].

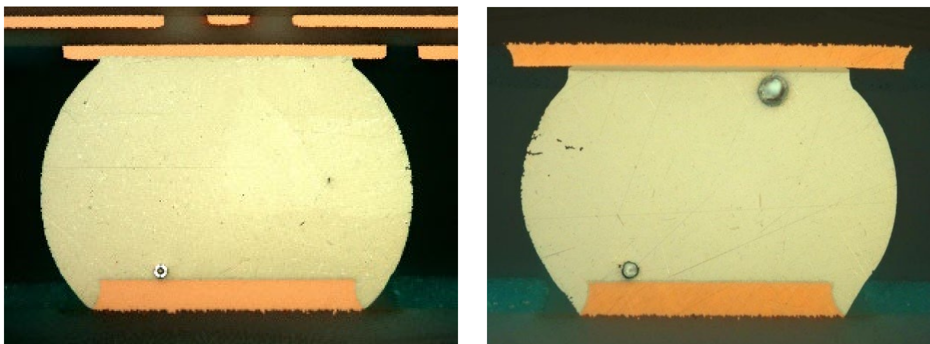

*Figure 16 - Cross-sections of solder joints with SMD pads on the component and NSMD on the PCB with a) the same solderable area on both sides and b) with reduced diameter of the solderable area with 15 % on the PCB side.*

## Solder composition

The intermetallic particles in SAC solders cause precipitation hardening of the solder. Therefore, SAC solders are harder and have higher strength than SnPb solders, but also slower creep. The slower creep normally leads to longer fatigue life of the solder joints compared to SnPb solder joints. When the lead-free solder consists of SAC305 (tin with 3.0 % Ag and 0.5 % Cu), the fatigue life is typically improved with 50-100 % compared to SnPb solders [82, 84, 85].

When SAC solder joints are aged, the IMC particles will grow in size at the same time as they will become fewer. This leads to a decrease of precipitation hardening. As a result, SAC solder joints will behave quite different when aged and/or have been exposed to thermal cycling compared to SnPb solder joints. If the high temperature extreme and the dwell times are

increased in thermal cycling, it has a much larger impact on SAC solders than on SnPb solders. Under such conditions, the fatigue life of lead-free solder joints may even become shorter than for SnPb solder joints.

Furthermore, exposure to high strain in solder joints has also a much larger negative impact on SAC solders than on SnPb solders since high strain will also enhance precipitation coarsening. Under such conditions, the fatigue life of lead-free solder joints may also become shorter than for SnPb solder joints [84, 86]. Factors that cause high strain are large CTE mismatch between components and the PCB, and large and fast temperature changes. Therefore, for BGA components that are only marginally larger than the chip, i.e. components with very restricted CTE, the fatigue life for lead-free solders may be only marginally higher than for SnPb solder or even shorter.

When a BGA solder joint is exposed to thermal cycling, recrystallisation of the solder will usually occur before cracks are formed. The recrystallisation will take place in the region having the highest strain and will result in the formation of small new tin grains (Figure 17).

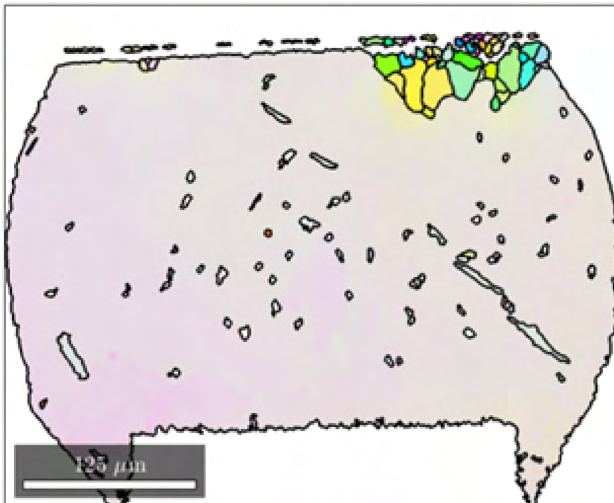


*Figure 17 - EBSD image of a cross-section of a solder joint to a BGA component showing a recrystallised region at the upper right corner.*

Cracks in the solder joints have been shown to be initiated already after less than 5 % of the fatigue life of the solder joints [87]. The fatigue cracks are usually initiated at a solder joint corner close to the interface of a solder pad and in most cases on the component side of the joint since the strain will be highest there.

The first initiated cracks are transgranular (through grains) with a very low growth rate [87, 88, 89], unless the strain is very high. Then after some time, the growth rate suddenly increases and continues to grow with about the same rate for the rest of the life of the solder joint (Figure ). Typically, this occurs after 20-50 % of the fatigue life and coincident with the completion of a recrystallised region across the high strain region of the joint [62, 90]. That is, tin grain recrystallisation precedes the faster crack propagation [88]. This has been found to be the case independent on component size (strain level) and testing conditions (temperature range and dwell time). The crack then propagates intergranularly (between grains) through the recry-

stallised region [54]. According to Mattila and Kivilahti [91], small cracks will simultaneously nucleate in the boundaries between the grains in the whole recrystallised region which eventually will coalesce into large cracks that propagate entirely through the solder joint.

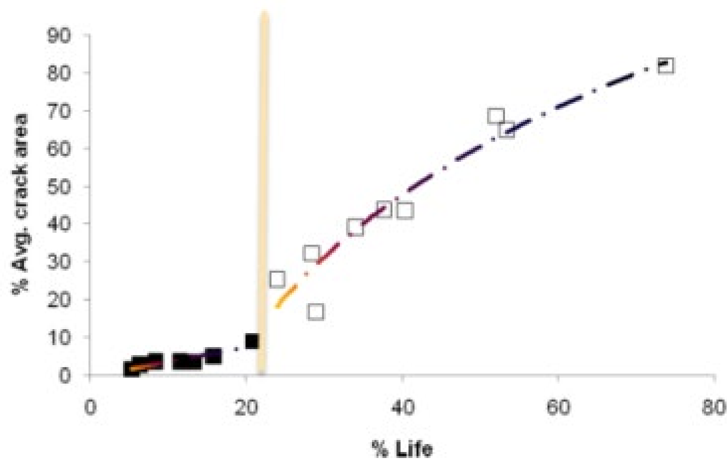


*Figure 18 - Crack initiation and propagation within a SAC305 joints in thermal cycling of BGA assemblies. The vertical line indicates approximately the stage of substantial recrystallisation inside the joints [92].*

Thus, according to Yin et al. [62], the formation of fatigue cracks in solder joints can be summarised in three stages as shown in Figure 19. In the first stage (a), precipitation coarsening will occur in the high strain region close to a solder pad. Slowly growing transgranular cracks are also initiated at joint corners. In the second stage (b), recrystallisation will occur all the way through the high strain region starting in the joint corners. In the recrystallised zone, a large number of randomly orientated tin grains will form between which an intergranular crack may grow faster than the initial transgranular crack. In the third stage (c), the cracks will propagate with a rather constant growth rate across the recrystallized region until a complete crack has formed.

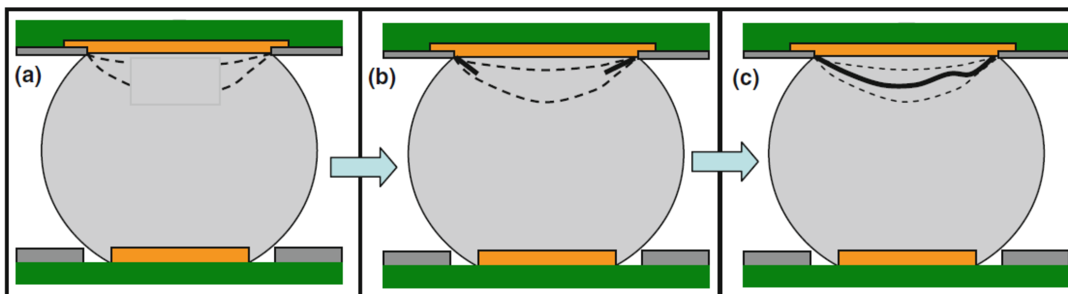


*Figure 19 - Stages for the formation of cracks in solder joints ta s BGA [62].*

It has been shown that the degree of precipitation hardening has a large influence on the number of cycles required for recrystallisation since small precipitates effectively act as barriers to the movement of dislocations [87]. Thus, a high degree of precipitation hardening may delay or even inhibit the development of recrystallisation [54, 62, 89]. Accordingly, the cycles to failure, $N_{failure}$ can be described with the equation

$$N_{failure} = N_{coars} + N_{recr} + N_{crack\ growth}$$

**where**

**$N_{coars}$ = Cycles needed to achieve enough coarsening for facilitating recrystallisation.**

**$N_{recr}$ = Cycles needed to achieve complete recrystallisation.**

**$N_{crack\ growth}$ = Cycles needed to achieve complete cracking.**

Off course, the various phases will to varying extent overlap but the split into these three phases are, nevertheless, useful for understanding how the fatigue life is affected by various factors.

New solders are now marketed that have been made more creep resistant by adding more elements to SAC solders, mainly bismuth, antimony, indium and nickel (see section 11.3). Besides enhancing the precipitation hardening, they also provide solid solution hardening. It can be expected that these solders will increase $N_{coars}$.

However, the increased solid solution and precipitation hardening of these solders are not entirely an advantage. The enhanced stiffness of the solders increases the risk for cracks forming in the PCB laminate and in ceramic capacitors but also for detachment of metallisation at terminations to ceramic capacitors [93].

## Grain structures in solder joints

The grain structure of lead-free solder joints may have a large impact on the fatigue of solder joints. Whereas the lead-rich phase in SnPb solder has isotropic properties, the tin-rich phase in both SnPb and SAC solders has anisotropic properties [55, 94]. That is, the material properties differ in various crystallographic directions (Figure 20). The CTE of pure tin grains at ambient conditions varies between approximately 15 ppm/°C (a- and b-axes) and 30 ppm/°C (c-axis), and the elastic modulus varies between approximately 22 GPa and 69 GPa [55. 60, 95]. Furthermore, both CTE and elastic modulus are highly dependent on temperature. At 125 °C, the CTE various between 20 ppm/°C and 40 ppm/°C and the elastic modulus between 15 GPa and 60 GPa [60]. Material properties for tin grains in SAC solders with embedded IMC particles have not been determined. The CTE is probably not too different from pure tin grains, but the elastic modules can be expected to be considerably higher due to precipitation hardening.

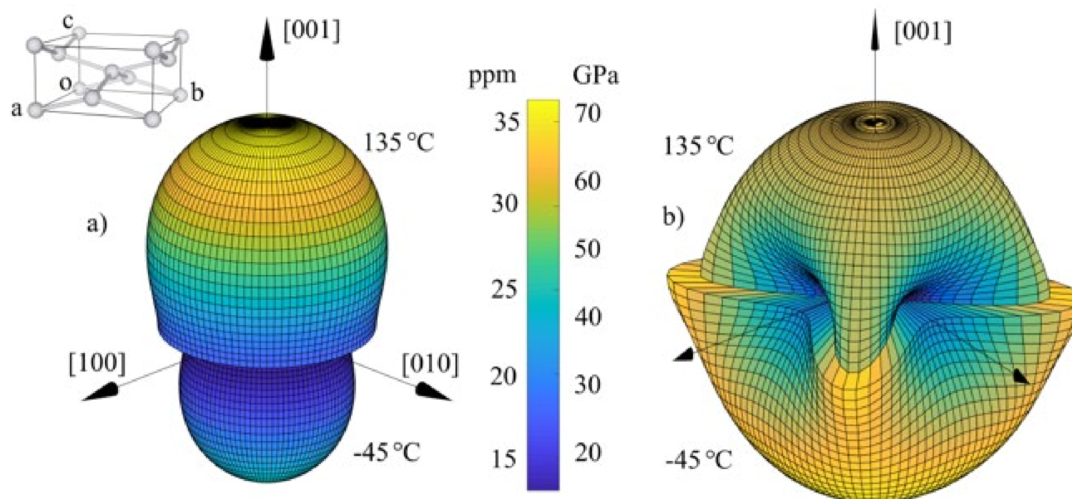


*Figure 20 - Surface representations of (a) the coefficient of thermal expansion and (b) the elastic modulus at -45 °C (lower half of the surface) and 135 °C (upper half of the surface) for β-tin [96].*

Since SnPb solder joints consist of a large amount of tin and lead grains mixed with each other, the soft and isotropic properties of the lead grains will mask the anisotropic properties of the tin grains. In contrast, SAC solder joints often consist of only one or a few large tin grains [53, 55, 60, 94, 97, 98].

The number of tin grains and the orientation of the grains in a SAC solder joint will have a large impact on the material properties of the solder joint. Several studies have shown that the orientation of the tin grains in the solder joints has a nearly random distribution [55, 94, 99]. Due to the anisotropic properties of tin grains, there may be a large difference in stress levels when exposed to thermomechanical stress, even for two neighbouring solder joints. As a result, the solder joint exposed to the highest stress level may be located randomly under a BGA, which may be far from the point of maximum shear stress for a corresponding BGA soldered with SnPb solder joints [100].

At ambient conditions, the CTE along the a- and b-axes in a tin grain (about 15 ppm/°C) is at the same level as the CTE of copper (16-17 ppm/°C) [60, 99, 101] and of the PCB laminate and BGA substrate in the x- and y-directions (about 12-18 ppm/°C) [99, 102, 103]. Therefore, if the tin grain in a single-grained solder joint is oriented with the a- and b-axes parallel to the board surface, the stresses at the interfaces at the solder pads will be low. On the other hand, since the CTE along the c-axis in a tin grain is about 30 ppm/°C, the CTE mismatch will be about 15 ppm/°C if the tin grain is oriented with the c-axis parallel to the board surface. Whereas the CTE of copper is fairly independent of the temperature [101] and probably also for the PCB, the CTE of tin is strongly affected by temperature. At 125°C, the CTE of tin is about 20 ppm/°C along the a- and b-axes and about 40 ppm/°C along the c-axis. That will result in a CTE mismatch to the pads of 20-25 ppm/°C at 125°C.

Consequently, single-grained solder joints with the c-axis parallel to the board surface have been shown to be much more prone to fatigue fractures during thermal cycling compared to solder joints with the c-axis perpendicular to the board surface, at least for BGA components with solder joints exposed to comparatively low strain [55, 60, 102].

Furthermore, if the solder pads on the BGA is located underneath the chip, the very low CTE of the chip will reduce the CTE of the component which will lead to an even higher CTE mismatch on the component side of the solder joints [55]. That will contribute to that most cracks in solder joints are formed on the component side.

For solder joints consisting of more than one grain, there will be an internal CTE mismatch between the grains which will depend on their orientation. The mismatch may be up to 15-20 ppm/°C, which will cause a high internal stress at the grain boundaries which will facilitate formation of fatigue cracks [55, 104].

Accordingly, the number of grains in the solder joints and the orientation of the grains will have large influence on the fatigue life of the solder joints [7, 96, 105, 106, 107]. Figure 21 shows a cross-section of three adjacent solder joints located in the second outermost row of solder joints to a BGA with SAC305 solder joints [96]. For the solder joint in the middle, there is a complete crack through the solder joint but no crack in the BGA laminate, while there are only small cracks in the surrounding solder joints but large cracks in the PCB laminate beneath the solder pads for these solder joints. The impact of cracks in the PCB laminate on the fatigue of the solder joints will be discussed in the section about the influence of PCB properties.

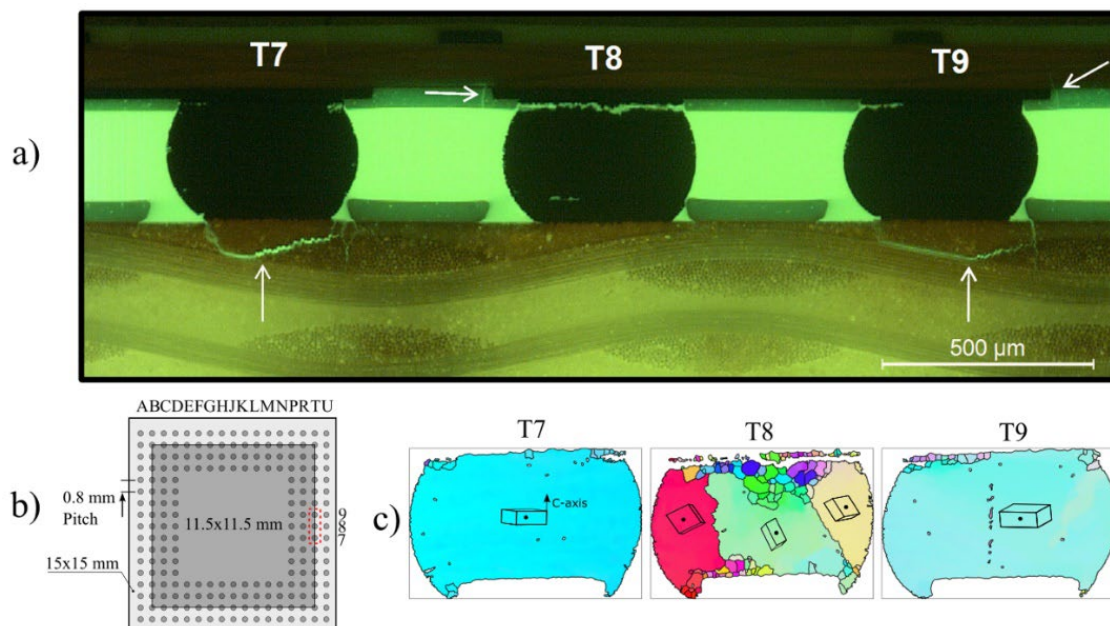


*Figure 21 - a) Cross-section of three adjacent solder joints to a BGA208 inspected with UV-light. b) Locations of the solder joints under the edge of the die as shown in the figure to the left. The component had been thermally cycled between −40 °C to 125 °C. c) Grain orientations of the joints in a).*

Examination of the solder joints using electron backscatter diffraction (EBSD) revealed that the two outermost solder joints were single-grained with the c-axis perpendicular to the board surface, while the solder joint in the middle had CT structure with three large grains (the small crystals have formed due to recrystallisation during thermal cycling).

That is, the two outermost solder joints will have a higher CTE in the direction perpendicular to the board surface compared to the solder joint in the middle. This will cause a large tensile stress on the two single-grained solder joint when temperature is decreased, and a compressive stress when temperature is increased. The opposite will be the case for the solder joint in the middle. These opposite tensile/compressive stresses on adjacent solder joints may explain why cracks formed in the PCB laminate under the single-grained solder joints. In the solder joint in the middle, the tin grains were oriented so the c-axes were more or less parallel to the board surface. Consequently, this solder joint was more prone to cracking in the solder joint. For BGA solder joints exposed to very high strain, such as BGA components with 0.4-0.5 mm pitch, the orientation of the tin grains has less influence on the fatigue of the solder joints [102].

Consequently, the solder joints to fail first in an array of SAC solder joints to a BGA component, which is not fine pitch, may be more or less randomly distributed as have been shown in several studies [94, 96, 100, 105, 197, 108]. Thus, the size and crystal orientation of the grain(s) in a SAC solder joint have a large impact of the fatigue life of the solder joint. While it is possible to predict which solder joints will be most likely to fail first for a BGA with SnPb solder joints based on a calculation of the shear strain that the solder joints will be exposed to, this is not possible for a BGA with SAC solder joints. The solder joint to fail first could be at almost any location of the package depending on the sizes and crystal orientations of the grains in the various solder joints. Furthermore, if a solder joint at a position exposed to most global expansion mismatch will have an unfavourable grain structure and grain orientation, it might lead to a very early failure.

Few studies have been conducted on how cracks are formed and grows in solder joints with interlaced twin structure, probably because solder joints with fully IT structure are not normally formed. They have mainly been reported to form in solder joints to land grid array (LGA) components. The interlaced twin structure in these solder joints have been found to be very resistant against fatigue cracking. Several studies have shown that if all solder joints to lead-free LGAs have this structure, the fatigue life may in fact be longer than for BGAs with the same dimensions [54, 109, 110]. For corresponding BGAs and LGAs having SnPb solder joints, the BGAs typically have 3 times longer fatigue life than the LGAs due to the higher stand-off of the BGAs [110].

As for solder joints having CT structure, recrystallisation needs to precede formation of cracks in the IT structure. However, the crack initiation in recrystallised IT structures appears to be delayed until complete recrystallisation of the solder joint has occurred and the recrystallised grains have grown substantially [111]. In addition, interlaced structures have more precipitates which are more evenly distributed than in cyclic twin structures [109, 111, 112]. This is probably due to the higher degree of undercooling required for interlaced twinning or be inherent to this microstructure. Anyhow, it renders the IT structure higher hardness and probably also more creep resistance than single-grained solder joints [109]. This will also ontribute to the resistance against crack formation.

Thus, the IT structure may contribute with a substantial improvement of the fatigue life although the fatigue life may not always be longer than for corresponding BGAs [53. 110]. According to Joshi et al. [110], there are unpublished industry reports that lead-free LGAs far from always perform that well. In an investigation performed by Arfaei et al. [53], they showed that solder joints to LGAs are not always fully interlaced. When evaluating the fatigue life of the solder joints with varying amount of IT structure in an accelerated thermal cycling test, the lifetime deteriorated as the percentage of interlaced solder joints decreased. Therefore, although interlaced solder joints may be beneficial for the fatigue life of solder joints, they may not improve or even be detrimental for the fatigue life of a component if not all solder joints are completely interlaced.

Although it is quite common with solder joints having mixed structure, few if any systematic studies have been carried out on how this structure affects the fatigue life of solder joints. However, a study performed by Barbini et al. gives some clues how it may affect the fatigue of solder joints [98]. They evaluated the fatigue life of solder joints to model area array components (die placed between two FR4 substrates). The components were produced with two different sizes of the packages and internal chips. The components had pitches varying between 1.0 mm and 2.2 mm as shown in Table 1. Solder balls attached to the components had three different solder ball diameters, 0.254 mm, 0.30 mm and 0.40 mm. The components were soldered to a PCB using only a flux.

Table 1 - *Dimensions of the components.*

| Body size | Chip size | Pitch |
|---|---|---|
| 14 mm x 14 mm | 12 mm x 12 mm | 1.0 mm |
| 14 mm x 14 mm | 12 mm x 12 mm | 1.2 mm |
| 21 mm x 21 mm | 18 mm x 18 mm | 1.4 mm |
| 21 mm x 21 mm | 18 mm x 18 mm | 1.8 mm |
| 21 mm x 21 mm | 18 mm x 18 mm | 2.2 mm |

The grain structure of the solder joints was single-grained or cyclic twin structure for solder joints with 0.40 mm solder balls, mainly single-grained or cyclic twin structure but with some mixed cyclic and interlaced twin structures for solder joints with 0.30 mm solder balls and mostly interlaced twin structure for solder joints with 0.254 mm solder balls.

They performed thermal cycling using three different thermal cycles: 0/100 °C, -20/100 °C and -40/125 °C, each cycle with 10 min dwells at the temperature extremes. The results from the thermal cycling tests are presented in Table 2 for components with 1.0 mm and 1.2 mm pitches, and in for components with 1.4 mm, 1.8 mm and 2.2 mm pitches. The solder joints having mixed structure are marked with yellow colour in the tables.

The results confirm that components which had IT structure (the solder joints with smallest standoff) had surprisingly long fatigue life and, in some cases, even longer fatigue life than the components with the highest standoff height that had SG or CT structures.

The solder joints with mixed structure had the best characteristic fatigue life (eta) for the components with 1.0 mm and 1.2 mm pitches (the small component). However, the beta values were very low resulting in fewer cycles to 1 % failure ($N_1$) compared to the solder joints having either dominating SG/CT structure or dominating IT structure.

For components with 1.4 mm to 2.2 mm pitch, the beta values were about the same independent of the grain structure, but now was the eta values considerably lower for the components having solder joints with mixed structure. Thus, also in this case was $N_1$ considerably lower for the components with mixed CT/IT solder joint structure.

Table 2 - *Summary of Weibull analyses for components with 1.0 mm and 1.2 mm pitches. N1 is the projected number of cycles for 1 % failure occurrence.*

| Ball diameter | Thermal cycle (°C) | 1.0 mm pitch | | | 1.2 mm pitch | | |
|---|---|---|---|---|---|---|---|
| | | $N_1$ (cycles) | Eta (cycles) | Beta | $N_1$ (cycles) | Eta (cycles) | Beta |
| 0.254 mm | 0/100 | 1 316 | 3 908 | 4.23 | 511 | 2 509 | 2.89 |
| 0.30 mm | 0/100 | 320 | 6 384 | 1.54 | 170 | 4 266 | 1.43 |
| 0.40 mm | 0/100 | 690 | 4 211 | 2.54 | 87 | 3 707 | 1.23 |
| 0.254 mm | -20/100 | 880 | 4 386 | 2.87 | 278 | 2 728 | 2.02 |
| 0.30 mm | -20/100 | 284 | 5 549 | 1.55 | 200 | 5 208 | 1.41 |
| 0.40 mm | -20/100 | 711 | 4 244 | 2.58 | 1265 | 2 984 | 5.36 |
| 0.254 mm | -40/125 | 339 | 1 917 | 2.66 | 149 | 1 356 | 2.09 |
| 0.30 mm | -40/125 | 173 | 2214 | 1.81 | 115 | 2 002 | 1.61 |
| 0.40 mm | -40/125 | 732 | 2 709 | 3.52 | 279 | 1 755 | 2.53 |

Table 3 - *Summary of Weibull analyses for the components with 1.4 mm, 1.8 mm and 2.2 mm pitch. N1 is the projected number of cycles for 1 % failure occurrence.*

| **Ball diameter (mm)** | **Thermal cycle (°C)** | **1.4 mm pitch** | | | **1.8 mm pitch** | | | **2.2 mm pitch** | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | **$N_1$ (cycles)** | **Eta (cycles)** | **Beta** | **$N_1$ (cycles)** | **Eta (cycles)** | **Beta** | **$N_1$ (cycles)** | **Eta (cycles)** | **Beta** |
| 0.254 | 0/100 | 365 | 1 516 | 3.23 | 202 | 789 | 3.38 | 82 | 446 | 2.76 |
| 0.30 | 0/100 | 205 | 699 | 3.75 | 136 | 404 | 4.24 | 73 | 303 | 3.25 |
| 0.40 | 0/100 | 4 101? | 1 291 | 4.02 | 264 | 938 | 3.63 | 151 | 653 | 3.15 |
| 0.254 | -20/100 | 468 | 1 500 | 3.95 | 141 | 799 | 2.65 | 59 | 380 | 2.47 |
| 0.30 | -20/100 | 144 | 526 | 3.56 | 135 | 350 | 4.84 | 32 | 254 | 2.24 |
| 0.40 | -20/100 | 381 | 1 270 | 3.82 | 270 | 802 | 4.23 | 131 | 656 | 2.86 |
| 0.254 | -40/125 | 144 | 815 | 2.66 | 103 | 461 | 3.07 | 28 | 201 | 2.36 |
| 0.30 | -40/125 | 110 | 394 | 3.60 | 66 | 192 | 4.31 | 47 | 172 | 3.57 |
| 0.40 | -40/125 | 216 | 862 | 3.33 | 169 | 474 | 4.47 | 54 | 322 | 2.59 |

Probably, the reason for the increased risk for early failures with mixed structure is that the part(s) with interlaced structure will be harder and more creep resistant than the part(s) with non-interlaced structure. As a result, this will likely increase the creep in the part(s) with non-interlaced structure that may lead to a shorter fatigue life of the solder joint, especially if these parts are located in a high-strain region. Since there will be a large variation in 1) the fraction of solder joints with mixed structure, 2) the locations and sizes of the interlaced parts in these solder joints, 3) the orientation of the grains in parts with SG/CT structure and 4) the location of these solder joints in the solder joint array, low beta values can be expected. Probably, the larger percentages of interlaced structures in the solder joints, the lower beta values.

## Moulding Compound

The main driving forces for fatigue of solder joints is the CTE mismatch between components and the PCB. Ideally, they should have the same CTE, but that is usually not possible to achieve. The CTE mismatch is especially important for lead-less components since they do not have leads that can reduce the stress on solder joints caused by changes in temperature.

For BGA and QFN components having chips with about the same size as the component, the CTE of the moulding compound will have a minor impact on the CTE of the components since it will mainly be determined by the stiff chip. However, for moulded components that have internal chips that are considerably smaller than the packages, the CTE of the moulding compound will have a major impact on the CTE of the components.

Previously, the moulding compounds that have been used for BGA and QFN components have had a CTE close to that of FR-4 PCBs. However, many semiconductor component manufacturers have gradually changed to new low CTE moulding compounds and a large percentage of the components have these moulding compounds today [113, 114]. There are several reasons for this change. The new moulding compounds consist of multiaromatic resin (MAR) and a high level of inorganic fillers. They reduce the absorption of water and thereby decrease the risk for "pop-corn" damages in components during soldering, which has become a larger problem with lead-free soldering. Thus, the change is, at least partly, caused by the transition to lead-free soldering, but there are also other reasons. Using these new moulding compounds, flame retardancy is achieved without additions of flame retardants, i.e. brominated flame retardants can be phased-out.

Due to the high degree of cross-linking and the high level of fillers, the moulding compound has considerably lower CTE and higher elastic modules than previously used moulding compounds [113, 114]. The lower CTE improves the chip reliability by minimising internal stresses in the component, but may endanger the reliability of solder joints between the component and a PCB. While the CTE of previously used moulding compounds (14-20 ppm/ºC) matched quite well the CTE of organic PCBs (15-18 ppm/ºC), the new compounds have a CTE in the range 6-10 ppm/°C. This can be compared with alumina used in ceramic components which has a CTE of about 7 ppm/°C.

Finite element modelling of BGA components with a full 27 x 27 array, and 0.5 mm, 0.8 mm and 1.27 mm pitches has shown that the new moulding compounds can decrease the fatigue life of the solder joints with 75 % to 87 % when reducing the CTE of the moulding compound from 16 ppm/°C to 7 ppm/°C (Table 4). The simulations were based on the use of SAC solder, 2.4 mm thick PCB and thermal cycling between 0 ºC and 100 °C. Unfortunately, the size of the internal chip was not given which complicate the interpretations of the results.

Table 4 - *Impact of a change of the CTE of the moulding compound on the characteristic life for a 27 x 27 full array BGA components with varying pitch [114].*

| **Pitch** | **CTE of moulding compound** | |
|---|---|---|
| | **16 ppm/°C** | **7 ppm/°C** |
| 1.27 mm | ~ 4 800 cycles | ~ 1 200 cycles |
| 0.8 mm | ~ 13 500 cycles | ~ 2 700 cycles |
| 0.5 mm | ~ 2 700 cycles | ~ 350 cycles |

Another study has been performed by Tee et al. [115]. They tested two different types of BGA components: one 16 mm x 16 mm $C^2$BGA240 and one 16 mm x 16 mm TFBGA240, both with a 5 mm x 5 mm chip and 0.8 mm pitch. The composition of the solder was not specified but it was most likely SnPb solder. Thermal cycling was performed between -40 °C and 125 °C.

The results from the study are presented in Table 5. There was a clear correlation between the CTE of the moulding compound and the characteristic life for both components. A decrease of the CTE of the moulding compound with 30 % caused a reduction of the characteristic life with about 30 %.

Table 5 - *The impact of a change of the CTE of the moulding compound on the characteristic life for two types of BGA components [115].*

| **Moulding compound CTE** | **Characteristic life** | |
|---|---|---|
| | **C²BGA240** | **TFBGA240** |
| 8 ppm/°C | 1 689 cycles | 1 443 cycles |
| 9 ppm/°C | 1 916 cycles | 1 630 cycles |
| 11 ppm/°C | 2 238 cycles | 1 941 cycles |
| 12 ppm/°C | 2 456 cycles | 2 145 cycles |

The type of moulding compound used in components for reliability evaluations is usually not specified. Therefore, it may be difficult to judge the relevance of reliability data presented in literature.

## PCB properties

The properties of the PCB will also affect the fatigue of the solder joints. The CTE in the plane parallel to the board surface will determine the CTE mismatch between a component and the PCB. This will be affected by the build-up of the PCB such as number of layers, thickness of the layers, type of resin, $T_g$, amount and type of filler, type of glass-fibre weave, amount of copper in the various layers and the types and number of interconnections between the layers.

The thickness of a PCB will affect the stress on the solder joints since a thicker PCB will be less compliant and will therefore give shorter fatigue life of the solder joints [74, 116].

Normally, routing vias are placed between solder joints to BGA components. On standard boards, the vias will be PTHs, whereas they will be µvias and possibly buried vias on high density interconnect (HDI) boards. According to Mawer and Levis, these vias, and especially PTHs, will constrain the expansion of the PCB in the z-direction and thereby increase the expansion in the x- and y-directions [85]. Furthermore, the interconnections will cause cutting of glass fibres in the glass weave. This could also be expected to increase the expansion in the x- and y-directions. Therefore, routing vias could be expected to increase the stress on solder joints and thereby impair the fatigue life of solder joints. However, an investigation of the effect of µvias and buried vias beneath a BGA showed that they improved the fatigue life of the solder joints with 10-20 % [14].

The high soldering temperature during soldering will cause some thermal break-down of the polymeric resins in PCBs. The thermal stability can be improved by using phenolic-based resins. They have both high $T_g$ and high $T_d$ (decomposition temperature) with low CTE due to a high degree of cross linking. A high content of inorganic fillers is usually added to the resin which will also contribute to reduced CTE, especially in the direction perpendicular to the board surface. It results in a laminate with a high elastic modulus but also a laminate that is more brittle than traditional low $T_g$ laminates [117, 118]. Consequently, less stress will be absorbed by these laminates when a solder joint is exposed to stress which will lead to a shorter fatigue life of the solder joint.

Large stress transferred to the PCB laminate may also cause cracks to form in the PCB laminate at and/or beneath solder pads, especially for laminates with a high content of fillers. Examples of such cracks formed in the PCB laminate at solder pads to various types of components during a temperature cycling test are shown in Figure 21 to Figure 23.

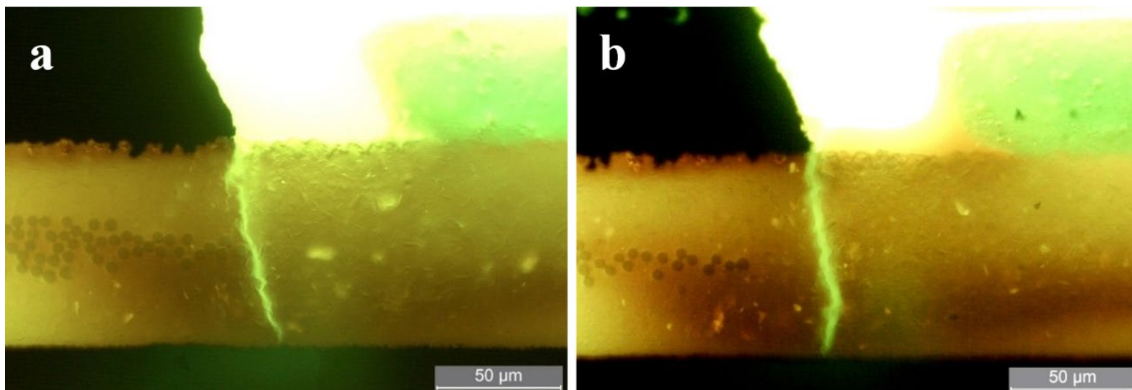


*Figure 22 Cracks formed in the laminate at solder pads to a) an LGA components and b) a 1206 ceramic resistor during a thermal cycling test [6].*

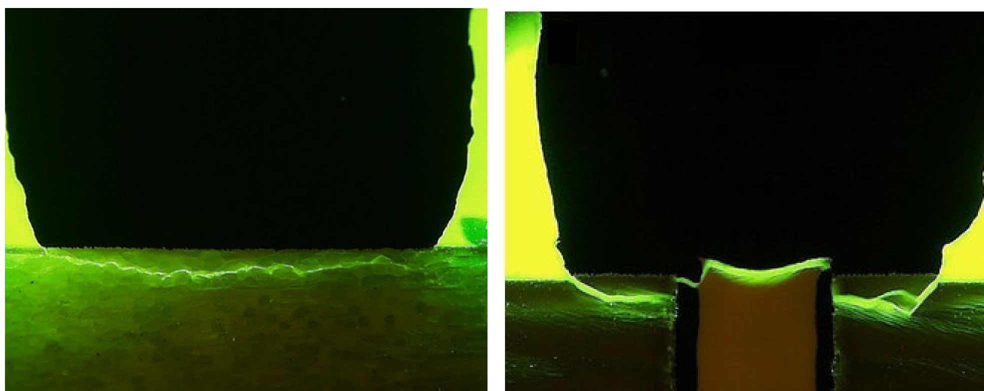

*Figure 23 Cracks formed in the laminate beneath solder pads to CBGA components during a thermal cycling test [119, 120].*

The higher the maximum temperature $T_{max}$ during thermal cycling, the larger risk for that cracks are formed in the PCB laminate. Laminate cracking may be quite extensive if thermal cycling is performed up to 125 °C but they may form to a lesser extent also if the maximum temperature is limited to 100 °C [6]. For some components, they may even form when the maximum temperature is limited to 85 °C [14].

Dudek et al. have examined the extent of cracks formed in the PCB laminate in a long-term thermal cycling test compared to thermal shock testing [121]. In the long-term test, thermal cycling was performed between 18 °C and 80 °C with a heating ramp of 1 hour, an upper dwell of about 20 min and a cooling ramp of about 6 hours, The total cycle time was 7.1 hours. The test was designed to be close to a characteristic service cycle environment. Thermal shock testing was performed in two chamber air to air cycling between –40 °C to 125 °C, -20 °C to 100 °C and -20 °C to 85 °C, all with a cycle time of one hour. Cracks were observed in the PCB laminate for boards that had been exposed to the thermal shock tests, and then especially in the test performed between –40 °C to 125 °C. No cracks formed in the PCB laminate in the long-term thermal cycling test.

If cracks are formed in the laminate beneath solder pads in a temperature cycling test, less stress will be transferred to the solder joints resulting in an improvement of the fatigue life of these [96, 105, 122]. Thus, if laminate cracking occurs in an accelerated temperature test, but not in a typical field environment, the fatigue life of solder joints from the test results may be overestimated.

See references 6 and 7 for a more extended discussion of how various factors affect cracking in the PCB laminate and how these cracks affect the fatigue life of solder joints.

## BGA substrate

The substrates in BGA components of OMPAC type is basically a PCB. The properties of a PCB that affects the reliability of solder joints will also be important for the substrates in BGA component. However, for BGA components an increased thickness of the substrates will be beneficial for the solder joint reliability since it will reducethe impact of the chip on the CTE of the component.

As for PCBs, cracks may form in BGA substrates during thermal cycling. Typical cracks formed in the substrate to a BGA component during thermal cycling are shown in Figure 24. These cracks will also reduce the stress on the solder joints leading to an overestimation of the fatigue life of the solder joints. They may also increase the risk of failure of the component due to humidity and contaminants penetrating in to the component.

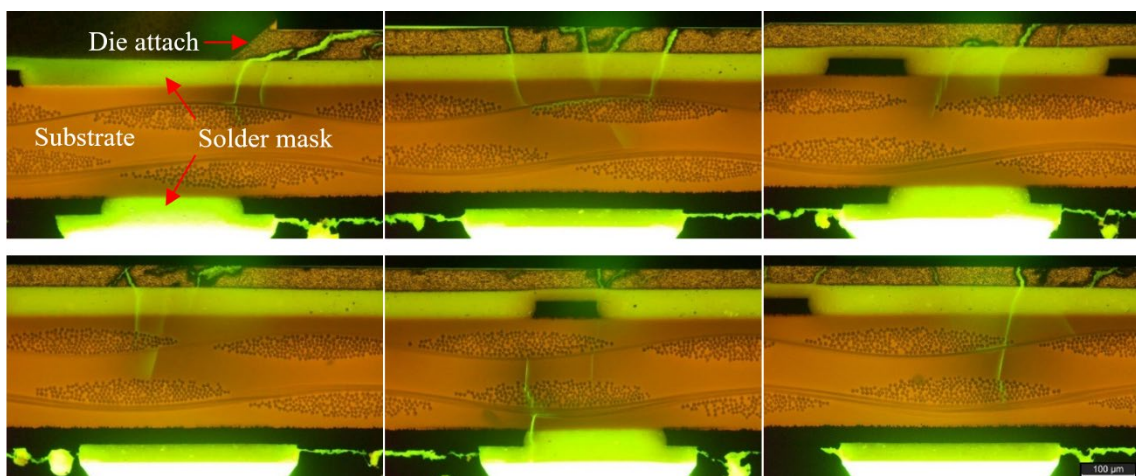


*Figure 24 Cracks formed in the substrate to a BGA176 during thermal cycling [14].*

## Underfills

For components having a large CTE mismatch toward a PCB, the reliability of solder joints can be improved by using an underfill. Underfills have been used for a long time to improve the reliability of flip-chips and has been a prerequisite for achieving acceptable reliability in many applications with flip chip technology. However, it is increasingly used also for BGA components and is probably necessary to use when having larger WLP components.

The improvement in solder joint reliability is achieved by filling the space between the components and the PCB with a material that should have a CTE close to the CTE of the solder and PCB. As described previously, solder joints can fail by two different failure mechanisms, brittle fractures and fatigue fractures of solder joints. Depending on which failure mechanism should be prevented, different underfills should be chosen.

Important underfill properties are CTE, modulus of elasticity and $T_g$ [123]. There are two kinds of underfills, low modulus underfills and high modulus underfills. If an underfill is used to prevent brittle cracks, for example due to a product being dropped on the floor, a low modulus underfill should be selected. However, these have a rather high CTE. Therefore, an underfill that give excellent results in a drop test may perform poorly in a thermal cycling test [124]. A wrong choice of underfill may reduce the fatigue life of the solder joints, in some cases with as much as four times [125].

To improve the fatigue life of solder joints, it is important that the underfill has as low CTE as possible. Since the base in underfills is an organic resin, usually epoxy, large amount of fillers needs to be added to the resin to reduce the CTE. This will increase the modulus of the underfill. Therefore, this type of underfill may degrade the reliability in drop tests.

The use of underfills has been reported to improve the fatigue life of BGAs 1.5 to 15 times [77, 126]. However, various underfills may perform very differently in various tests and for various component types and it is important to choose the right underfill for a specific component [127].

Underfills can be applied using either capillary underfill or fluxing underfill [128]. Capillary underfills are dispensed and cured after soldering. The dispensing is done along two perpendicular sides of the component and the underfill is sucked in under the component due to capillary forces. Fluxing underfill is dispensed at the component site prior to the placement of the component. No solder paste is printed on the solder pads. The underfill act as flux during the soldering process and is at the same time cured. It is mainly used for improvement of the resistance against brittle fractures.

## Conformal coatings

Conformal coatings are applied to improve reliability of assemblies used in humid and harsh conditions. Something not mentioned in J-STD-001, which ought to have been mentioned, is that applying a conformal coating often comes with a price. The price to be paid is an increased risk of shortening the fatigue life of solder joints, especially to area array and QFN components. If coating material penetrate in underneath components and completely fills the space underneath the components at some locations, the larger CTE of the coating material compared to the solder will increase the stress on the solder joints when exposed to changes in temperature.

Sytsma and Wrightson have reported that the fatigue life of a QFN44 component was reduced from about 2200-2400 cycles without coating to about 300-750 cycles with an acrylic coating, a decrease with 70-85 % [129]. The test they used was a thermal shock test using a two-chamber equipment with the upper temperature at 125 ºC and the lower temperature at -55 °C and a total cycle time of 44 minutes.

To prevent that conformal coatings penetrate in underneath area array and QFN components, some companies require a conformal coating free area around these components. However, that means that there will be no environmental protection of the interconnections underneath these components.

### 9.5.2 Solder joints to bottom termination components

A thorough guideline for design and assembly process implementation for bottom termination components can be found in IPC standard IPC-7093 [32].

Bottom termination components (BTCs) have external connections that consist of metallised terminations that are an integral part of the component body [32]. It includes land grid array components (LGAs) and quad flat no-lead (QFN) types of components.

#### Land grid array components

Land grid array components are basically BGA components with no attached solder balls. The only solder in the connections between an LGA component and a PCB will come from the printed solder paste used to solder the assembly. Consequently, the stand-off of the component will be considerably lower than for BGA components resulting in much higher strain in the solder joints when exposed to thermomechanical stress. This may cause a much shorter fatigue life of the solder joints, but that is not always the case for LGAs soldered with lead-free solders due to a different morphology of the solder joints (see section about grain structures in solder joints).

#### Quad flat no-lead types of components

Flat no-lead components have terminations along the perimeter on two sides (dual flat no-lead DFN) or all four sides of the package (quad flat no-lead – QFN). They usually have only a single row of leads along the periphery, but they may have multiple rows. The die attach pad is exposed on the bottom of the package and can be soldered to the PCB in order to achieve an efficient heat path. The components can be split into full lead package and lead pullback package (Figure 25). The full lead package has the whole lead exposed at the side of the package whereas the lead pullback package has only the top half of the lead exposed at the side of the package.

*Figure 95 - Cross-sections of leads to QNF components having full lead (left) and lead pullback (right) design.*

Since the QFN components do not have solder balls, the stand-off will be much lower than for BGA components. As for LGA components, this results in much higher strain in the solder joints to a QFN in a thermal cycling test compared to a BGA and, consequently, in a shorter fatigue life for a QFN component compared to a BGA component with the same chip and package sizes.

For QFN components having only one row of leads along the periphery, the solder joints are not located beneath the chip (chip shadow) but, if the chip is almost of the size of the component, the solder joints will be close to the chip edge. Therefore, chip to component length ratio will have a large impact on the fatigue life of the solder joints and is more important for the fatigue life than the chip size itself. Figure 26 shows the fatigue life as a function of chip (die) to component length ratio reported by Chan et al. [130]. The evaluated QFN components had body sizes of 5 mm to 9 mm and were thermally cycled between 0 ºC and 100 ºC. It can be noted that SnPb solder joints performed better than SAC305 as could be expected due to the high strain in solder joints to QFN components.

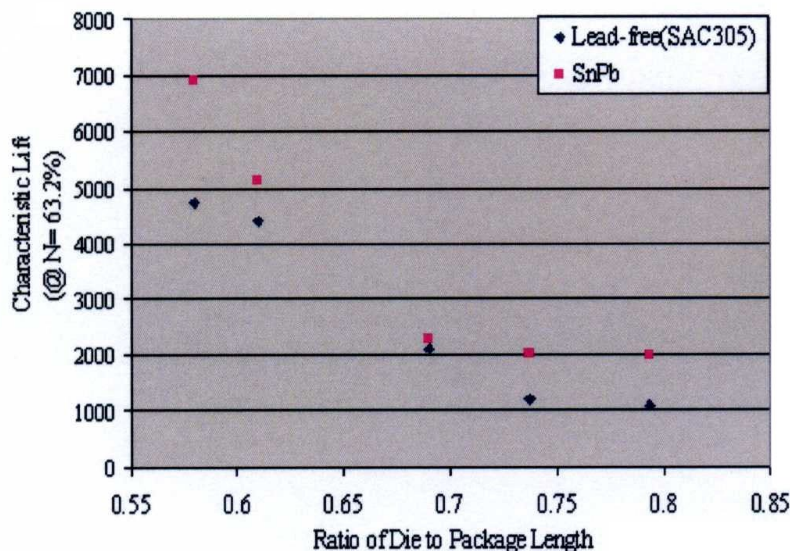


*Figure 26 - Impact of ship to component length ratio on the fatigue life for QFN components evaluated by Chan et al. [130].*

A similar evaluation has been performed by Syed and Kang [131]. The evaluated QFN components in that evaluation were soldered using SnPb solder, had body sizes of 7 mm to 12 mm and were thermally cycled between -55 ºC and 125 ºC but with only 2 minutes ramps. The results from that evaluation are shown in Figure . Although it is difficult to compare the absolute values due to different test conditions and $N_f$ values, the trend for the two evaluations is very similar.

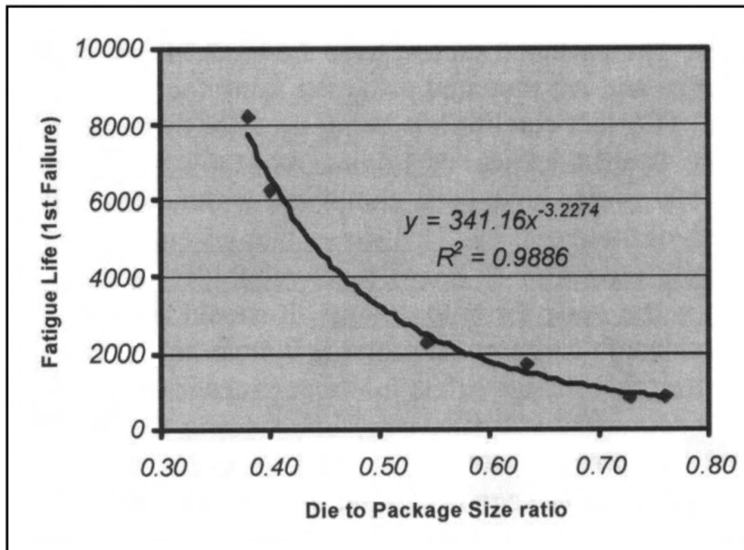


*Figure 27 - Impact of ship to component length ratio on the fatigue life for QFN components evaluated by Syed and Kang et al. [131]*

Smetana et al. compared the fatigue life for a QFN72 with body and chip sizes of 10 mm and 3.2 mm, respectively, with a QFN64 with body and chip sizes of 9 mm and 7.62 mm, i.e. a ratio of 0.85 [84]. When soldered with SAC305 and cycled between 0 ºC and 100 ºC, the QFN72 had an eta value of 5 114 cycles whereas the QFN64 had an eta value of only 163 cycles, a difference in eta values of a factor of about 30. That is, the smaller component had a much shorter fatigue life.

QFN components may have several internal chips which then normally are asymmetrically placed in the component. The distance between the solder joints and the chips will then be rather short to some of the solder joints. Thus, even if the chips may be rather small, their asymmetrical placement can be expected to have a large negative impact on the fatigue life of the solder joints. The asymmetric placement of the chips may also cause warpage of the component that may also have a negative impact on the fatigue life of the solder joints [32].

One of the most important factors for the fatigue life of solder joints to a QFN component is the stand-off of the component [32]. For QFN components with a thermal pad, the stand-off will mainly be determined by the solder joint formed to the thermal pad.

The exposed leads on the bottom side of the components are plated with a surface finish to preserve the solderability. However, exposed lead surfaces at the sides of the component are usually bare copper. Therefore, the solderability of the exposed side of the leads will degrade rather rapidly which may lead to rather poorly formed solder fillets. According to Syed and Kang [131], failure to wet the sides of the leads may cause a reduction of the fatigue life with 50 % for components with large chip to component length ratio, less for components with smaller ratio. Consequently, to achieve properly formed solder fillets the wettability of the leads is important. The capability to wet the leads on the sides of the components may be affected by the stand-off of the component. An increase of the stand-off, which is beneficial for the fatigue life of the solder joints, will make it more difficult to wet the leads on the sides of the component. Although it is pointed out in IPC-7093 that it is beneficial to form a solder fillet to the leads

on the sides of the component, it is not requiredin J-STD-001, and it is almost impossible to achieve for components with lead pullback.

As for BGA components, the properties of the moulding compound for QFN components may have a large impact on the fatigue life of solder joints, but experimental data are scarce. Syed and Kang tested a QFN produced with 8 moulding compounds [131]. The component used for the evaluation was a 7 mm x 7 mm QFN48 with a 3.8 mm x 3.8 mm chip and it was soldered to a 1.6 mm thick PCB using SnPb solder. The test boards were thermally cycled between -55 ºC and 125 ºC with 2 minutes ramps. The results from the evaluation are presented in Table 6. Generally, the eta values decreased with decreasing CTE of the moulding compound. The discrepant result for compound 2 may be due to the lower $T_g$ for that material, which actually was lower than the upper temperature in the thermal cycling test.

Table 6 - *Mould compound properties and test results for a QFN48 produced with various moulding compounds [131].*

| **Mould compound** | **CTE (ppm/°C)** | **$T_g$ (°C)** | **Modulus (kg/mm$^2$)** | **1$^{st}$ failure (Cycles)** | **Eta (Cycles)** |
|---|---|---|---|---|---|
| 1 | 7 | 125 | 2 650 | 649 | 978 |
| 2 | 7 | 120 | 2 710 | 2 166 | 3 150 |
| 3 | 8 | 130 | 2 650 | 1 219 | 2 384 |
| 4 | 9 | 150 | 2 800 | 2 700 | 3 822 |
| 5 | 10 | 135 | 2 400 | 3 747 | 5 320 |
| 6 | 11 | 135 | 2 400 | 3 578 | 4 708 |
| 7 | 12 | 130 | 1 900 | 4 218 | NA |
| 8 | 14 | 185 | 1 800 | 3 684 | 5 090 |

### 9.5.3 Solder joints to ceramic resistors

Cracks in solder joints to ceramic resistors are initiated underneath the component, either at the corner of the component or at the innermost part of the solder joint [132]. The cracks grow quickly under the component and then continue at a slower speed through the solder fillet.

### 9.5.4 Solder joints to components with leads

For surface-mounted components having leads such as QFP and SOIC components, the leads will act as springs that will reduce the stress on the solder joints. Therefore, leaded components normally have very long fatigue life. An exception is leaded components with low stand-off and wide leads.

The type of surface finishes on the component leads may also have an impact on reliability. Components with leads generally has pure tin as lead-free surface finish. The main risk with this surface finish is growth of whiskers (see section 9.8.4).

## 9.6 Brittle fractures in solder joints

There are a number of factors affecting the risk for formation of brittle fractures in IMC layers to solder pads of which the most important are:

- The type of stress applied to solder joints.
- Composition and mechanical properties of the solder.
- Thickness and composition of intermetallic layers.
- Properties of components and PCBs.
- Design of solder pads on components and PCB.

After soldering, there will be large residual stresses in the solder joints due to the CTE mismatch between components and the PCB. The degree of precipitation hardening will also be the highest immediately after soldering. Due to these residual stresses and the high degree of precipitation hardening, solder joints are most prone to brittle fractures in IMC layers directly after soldering. However, the residual stresses will slowly decline as a result of creep in the solder, and the precipitation hardening will slowly decrease due to precipitate coarsening. That is, with time, the susceptibility to brittles fractures will decrease.

High susceptibility to brittles fractures is characteristic for lead-free soldering. Tin-lead solder joints creep much faster, and they are also to a much lesser extent affected by precipitation hardening. Consequently, SAC-solders with low silver-content (1% or less), which has less precipitation hardening than SAC solders with higher content of silver, are often used for applications with high risk for brittle fractures, for example portable products. The price to be paid for that is in many cases a shorter fatigue life of the solder joints. Another reason for increased risk for brittle fractures is that thicker and more complex intermetallic layers may form when lead-free solders are used (see section 9.2 and references 2 and 66).

During the past 10 years, new lead-free solders have been developed that have been made more creep resistant by increasing the degree of precipitation and solid solution hardening (see section 11.3). It can be expected that they increase the risk for brittle fractures in the IMC layers since they have a higher elastic modulus, although it will also depend on the composition of the IMC layers formed with these solders.

Activities that may cause bending of the assemblies is most likely to cause brittle fractures since bending may cause both high strain and high strain rate. Therefore, it is important to ascertain that solder joints are not exposed to too high strain levels during manufacturing and handling. IPC has together with JEDEC developed the standard IPC/JEDEC-9704, Printed wiring board strain gage test guidelines, for how to verify that [133].

Brittle fractures caused by bending has been reported to occur under several conditions such as [134, 135, 136 137]:

- In-circuit testing.
- Depaneling or breaking of end tabs.
- Insertion or removal of boards in chassis.
- Attachment or removal of fasteners, press-fit connectors, and spring-loaded heat sinks.
- Keypad actuation.
- Shipping or handling with insufficient mechanical support.
- Dropping a product to the ground (probably one of the most common situations causing brittle fractures).

The tensile strength of solder decreases with increasing temperature which will lead to more plastic deformation in the solder when exposed to stress [138]. This may result in reduced risk for fractures in the intermetallic layer when the temperate is increased under condition that the tensile strength of the IMC layer is not also reduced. Therefore, fracturing in solder joints may change from brittle fracture in the IMC layer to ductile fatigue fracture in the bulk solder if temperature is increased and the opposite if temperature is decreased.

Brittle fractures may also form when products are exposed to temperature or power cycling [134, 139], mechanical shock [140, 141, 142] and vibration [143, 144]. As mentioned before, a failure due to a brittle fracture may be the result of one single highstrain event or many consecutive events at a lower strain level. The most severe stress due to changes in temperature occurs during soldering processes. Due to the different CTE for components and PCBs, the solder joints will be exposed to both high strain and high strain rate in the cooling phase during soldering. The crack shown in Figure 7 was initiated during cooling after soldering of a large PBGA (45 mm x 45 mm). Once initiated, it can easily continue to grow if the solder joint is exposed to low-strain events.

Thus, brittle fractures may occur already under the cooling phase during a soldering process, but they may also occur under the heating phase in a second soldering process. An example of a brittle fracture that occurred during a second soldering process is shown in Figure 28.

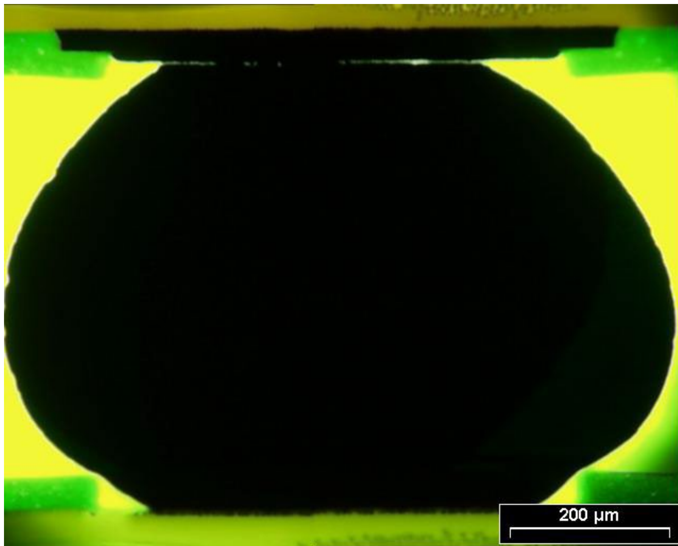


*Figure 28 - Cross-section of a solder joint to BGA that has passed a second reflow soldering process. The sample has been moulded in epoxy with an added fluorescent agent and has been examined using UV-light.*

The figure shows a cross-section of a solder joint to a BGA with eutectic tin-lead solder which displayed intermittent failures after it had passed a second reflow soldering process. The BGA has four peripheral rows of solder joints and the figure shows one of the solder joints in the inner row. As shown in the figure, the solder does not wet to the solder pad on the component. The shape of the solder joint indicates that it has melted during the second soldering process. Most likely, the outer rows of solder joints melted first, and all stress caused by the increased temperature was concentrated on the solder joints in the inner row that had still not melted. This caused a brittle fracture at the pad interface for the solder joint shown in Figure 28. Then the solder melted. Since no flux was present and an intermetallic layer probably covered the fractured surface, the molten solder failed to wet the pad surface. This type of failure has also been reported by Silk et al. [145].

See reference 66 for a more extended discussion of the impact of IMC layers on the risk for brittle fractures.

## 9.7 Electrochemical migration

**Electrochemical migration (ECM) is defined** in IPC-TR-476 [146] as "*the growth of conductive metal filaments on a printed board under the influence of a DC voltage bias. This may occur at an external surface, an internal interface, or through the bulk material of a composite. Growth is by electro-deposition from a solution containing metal ions which are dissolved from the anode, transported by the electric field and redeposited at the cathode*".

The redeposited metal ions will form tree-like metal filaments called dendrites. These will grow towards the anode where the metal ions come from and, with time, may cause a short circuit when they reach the anode (Figure 29).

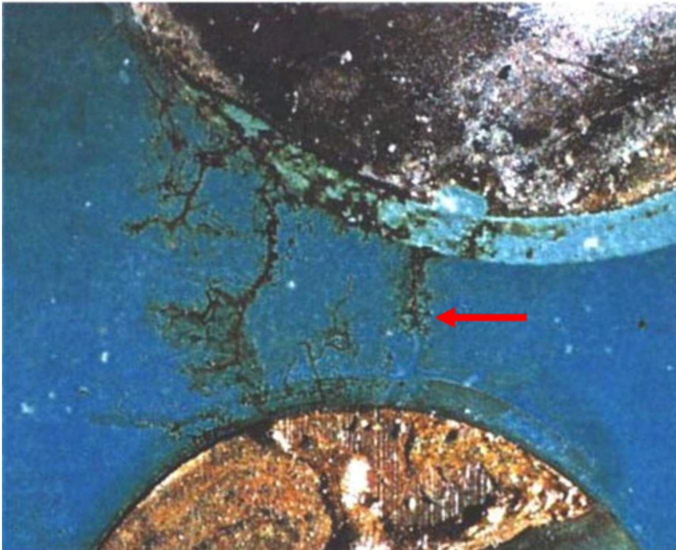

Figure 29 - *Dendrites formed on an assembly exposed to condensation when biased. The dendrite to the right (marked with a red arrow) has caused a short circuit and has been partly blown away by the resulting electric discharge.*

Three requirements need to be met to facilitate ECM:

- DC voltage biased electrodes.
- A medium in which ions can migrate.
- Substances that can form ions.

Electrochemical migration will only occur between biased electrodes, but a few volts are enough to make ECM possible.

Since the failure mechanism includes migration of ions, there must be a medium between the electrodes that enables migration of ions. The medium consists normally of a water film. Therefore, ECM does not normally occur in dry conditions. However, other mediums that may promote ion migration are possible. For example, it has been reported that ECM has occurred in organic flux residues.

When electronic products are used in humid environments, water will be adsorbed[6] on most surfaces. The amount of water adsorbed will depend on temperature and relative humidity, but also on properties of the surfaces. More water will be adsorbed on hydrophilic surfaces compared to hydrophobic surfaces. When the surface consists of a polymeric material, this material may also absorb water.

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[6] Adsorbed water is water that has added to the surface of a material whereas absorbed water is water that have diffused in to the material.

Hygroscopic contaminants on the surface may also affect the thickness of the adsorbed water film. At or above a critical relative humidity, many salts absorb water forming a saturated solution of the salt. Thereby, the thickness of the absorbed water film is greatly increased. The dissolved salt will also contribute with ions that will increase the electrical conductivity and promote ECM. In Table 7, the critical relative humidities at which this happens are given for a number of halide-containing inorganic compounds (which may originate from process and flux residues).

Table 7 - *Critical relative humidities for a number of inorganic compounds at which saturated solutions are formed [147, 148].*

| Compound | Temperature (°C) | Relative humidity (RH) (%) |
|---|---|---|
| $LiCl \cdot H_2O$ | 20 | 15 |
| KF | 100 | 22.9 |
| NaBr | 100 | 22.9 |
| $CaCl_2 \cdot 6H_2O$ | 24.5 | 31 |
| $CaCl_2 \cdot 6H_2O$ | 5 | 39.8 |
| KBr | 100 | 69.2 |
| NaCl | 10-40 | 75 |
| KCl | 5-25 | 84 |
| KBr | 20 | 84 |
| NaF | 100 | 96.6 |

Anderson et al. [149] have shown that the resistivity of a surface contaminated with a hygroscopic compound decreases dramatically when the relative humidity is increased to values above the critical relative humidity for the hygroscopic compound. The resistivity is then rather little affected by a further increase in relative humidity. For an assembled PCB, the surface would be contaminated with a mixture of contaminants from various process steps having varied critical relative humidities. Therefore, the surface resistivity for an ordinary production assembly can be expected to decrease more or less gradually with increasing relative humidity.

Not only ionic compounds may have hygroscopic properties. Polyglycols and many other types of organic non-ionic surfactants common in some types of fluxes and fusing oils are very hygroscopic even at relative humidities down to almost 0 % [150]. When present alone, they contribute to a decrease of the surface resistivity mainly by increasing the thickness of the adsorbed water film. Since they do not contribute to ionic conduction, the decrease of surface resistivity is rather small. What makes them hazardous is the fact that they promote a dissolving

medium for ionic contaminants with low hygroscopicity that would otherwise be rather harmless except at very high relative humidities. Thereby, strong synergistic effects may be observed when hygroscopic non-ionic compounds are mixed with ionic compounds of low hygroscopicity. For example, as shown in Table 8, a mixture of polyethylene glycol and adipic acid (a common ingredient in halide-free fluxes with very low hygroscopicity) has the same impact on SIR as sodium chloride [151]. The figures in Table 9 also show that ionic compounds have negligible impact on SIR at relative humidities below the critical relative humidities for the compounds. The reason why NaBr and KCl do not have an impact on the surface conductivity despite a critical RH below that at which the measurements were performed may be due to that surface dispersed chemicals have lower critical RH than the bulk salts [151].

Table 8 - *Surface conductivity measured at 35 °C and 90 % RH for copper comb patterns on FR-4 substrate contaminated with various compounds [151].*

| Compound | Added amount ($\mu g/cm^2$) | Surface conductivity ($ohm^{-1}$) | Critical RH[1] (%) |
|---|---|---|---|
| **NaCl** | 2.00 | $1.3 \times 10^{-8}$ | 76 |
| **NaF** | 1.44 | $4.0 \times 10^{-11}$ | 97 |
| **NaBr** | 3.52 | $3.8 \times 10^{-11}$ | 84 |
| **KCl** | 2.55 | $3.1 \times 10^{-11}$ | 84 |
| **$MgCl_2$** | 1.63 | $2.9 \times 10^{-8}$ | 44 |
| **$CaCl_2$** | 1.90 | $9.5 \times 10^{-8}$ | 29 |
| **Adipic acid** | 5.00 | $2.7 \times 10^{-11}$ | 99.6 |
| **PEG 400[2]** | 13.70 | $3.2 \times 10^{-10}$ | 0 |
| **Adipic acid + PEG 400** | 5.00 + 13.70 | $1.4 \times 10^{-8}$ | - |
| **None (Reference)** | 0.00 | $3.5 \times 10^{-11}$ | - |

*1 Calculated values.*

*2 PEG 400 = polyethylene glycol with a molecule weight of 400.*

Fortunately, not all contaminants are hazardous. Some are even beneficial. Rosin, a common base in many fluxes, is hydrophobic, i.e. water repellent [150]. Therefore, rosin residues decrease the amount of water adsorbed on the surface and thereby improve the surface resistivity. Rosin residues may also encapsulate ionic contamination and thereby immobilise ions. In addition, water that condenses on a hydrophobic surface tends to form isolated droplets as water does on a greasy surface. Thus, even if condensation occurs, rosin residues improve the situation.

In non-condensing environments, ions must be present on the surface for ECM to occur. However, if water condenses on the surface, or if water droplets fall on an assembly, ECM may occur within a few seconds even if the surface is clean. Due to the intrinsic ionisation of water into hydrogen and hydroxide ions, a water film has always some conductive properties. This may be further enhanced by adsorption of some gases from the atmosphere that form ionic compounds with water, for example carbon dioxide. The bias will then start producing metal ions by oxidation of the anode which will quickly increase the ion content in the water film and ECM will take place.

Although IPC define ECM as the growth of conductive metal filament, the metal filaments cannot start to grow until metal ions have formed at the anode and then migrated to the cathode. That is, the growth of the metal filament is only a part of the process, and it can only occur after the electrode processes have been going on for some time. In fact, failures may occur due to low surface insulation resistance before the metal filaments start to grow. Therefore, it is not adequate to limit the definition of ECM to the growth of metal filament. A better definition would be "*current leakage due to electrochemical reactions on a printed board under the influence of a DC voltage bias that might involve the growth of conductive metal filaments*".

See reference 3 for a more extended discussion of this topic.

### 9.7.1 Creep corrosion

Creep corrosion is a failure mechanism that can be mistaken as ECM. Although the creep corrosion products may have an appearance similar to dendrites formed due to ECM, there are several differences. Whereas dendrites consist of metal filaments, creep corrosion products consist mainly of copper sulphide. Furthermore, dendrites are grown under the influence of a DC voltage bias and are therefore always grown between biased surfaces. In contrast, creep occurs in all directions and does not require the board to be powered [152].

Surface finishes with immersion silver (ImAg) and OSP, have been reported to be most prone to form creep corrosion, but it has been reported also for ENIG. Creep corrosion products on PCBs with ImAg consist primarily of $Cu_2S$ with a small amount of $Ag_2S$ [153, 154, 155, 156]. Creep corrosion products formed on ENIG consist mainly of $Cu_xS$ [157].

According to Schueller [153] and Chao et al. [156], it appears that $Cu_2S$ is being formed in a layer of moisture on the surface and precipitates out of solution as it forms (since $Cu_2S$ is insoluble in water). For boards with OSP surface finish, creep corrosion sometimes seems to have grown in waves with layers of corrosion products grown on top of each other and where the layers gradually become smaller and smaller.

## 9.8 Interconnect failures in PCBs and components

### 9.8.1 Plated through hole cracking

In an FR-4 PCB laminate, a glass weave is used to restrict the CTE in the x-y plane to about 16-18 ppm/°C. Since the polymeric resin in the PCB laminate has a much larger CTE (about 45 ppm/°C at temperatures below $T_g$), it will cause a much larger CTE along the z-axis in the laminate, typically 50-60 ppm/°C at temperatures below $T_g$ and about five times higher above the $T_g$. Barrels in printed through holes consist of copper that has a CTE of 17 ppm/°C.

Thus, an increase in temperature will cause stress on the PTH barrels which may result in fractures in the PTH barrel. Furthermore, the hole plating will act as a rivet in the laminate. This may result in pad lifting of annual rings [158]. The interconnections between barrels and conductors in inner layers may also be affected resulting in interconnection failures to conductors in the inner layers. The various types of failures are shown in Figure 30.

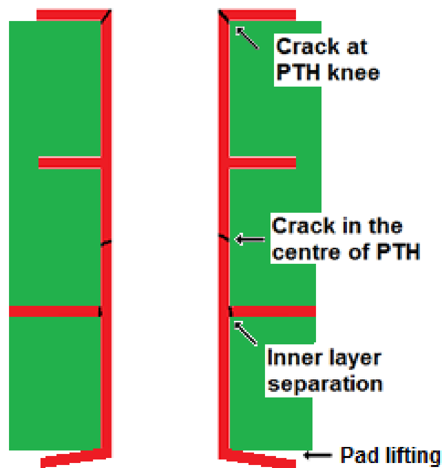
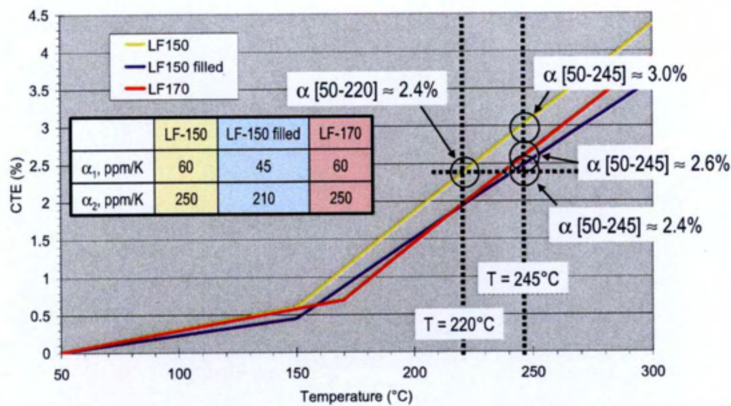



*Figure 30 - Failure sites in a PTH.*

The most important factor affecting cracking of PTH barrels and interconnection failures to inner layers is temperature changes. The larger the temperature change, the greater the risk for failures. Hence, soldering processes entail the greatest risk for these types of failures. Due to the transition to lead-free soldering and the resulting increase in soldering temperatures, the stresses on PTH barrels and interconnections to inner layers have increased during soldering. Hence, there has been a need to change the properties of the PCB laminate to decrease the stress levels during soldering.

The two main material properties of the resin affecting the stress levels are CTE and $T_g$. A decrease of CTE will decrease the stresses during soldering. This can be achieved by adding inorganic fillers to the resin, for example silica ($SiO_2$) or alumina ($Al_2O_3$), which have very low CTE. However, fillers will not only affect CTE but also electrical properties like $D_f$ and $D_k$ and mechanical properties like fracture toughness and adhesion strength to other materials. An increase of $T_g$ will also reduce the stresses during soldering since it will reduce the temperature range where the resin has very high CTE. The $T_g$ can be increased by increasing the degree of cross-linking in the resin which may also decrease the CTE slightly. Thus, by using laminates with higher $T_g$ and/or added fillers, the total expansion of the PCB in the z-direction during soldering can be kept at the same level in lead-free soldering as previously in tin-lead soldering (Figure 31)




| | LF-150 | LF-150 filled | LF-170 |
|---|---|---|---|
| $\alpha_1$, ppm/K | 60 | 45 | 60 |
| $\alpha_2$, ppm/K | 250 | 210 | 250 |

*Figure 31 - Schematic effect of Tg and filler on the thermal expansion before and after Tg [159].*

Failures in PTHs may also occur due to large temperature variations in field conditions. Although the temperature change then is much lower than in soldering, a large number of temperature cycles may cause fatigue failures of the barrels. Also bending of PCBs may cause stresses on the PTH barrels, but these stresses are more likely to cause interconnection failures to inner-layers than cracking of PTH barrels. Since $T_g$ normally is higher than use temperatures, it is only affecting the stress levels during soldering processes.

Another very important factor affecting the reliability of PTH barrels is the quality of the platings in the holes. The walls in the drilled holes should be smooth and the plating should have an even thickness without any defects. When ENIG is used as surface finish on the PCB, the copper plating in the PTH may be coated with about 5 µm electroless Ni. Since electroless Ni is much stronger and less elastic than copper, this will strengthen the hole plating and thereby decrease the risk for cracks in the PTH barrels but increase the risk for interconnection failures to inner layers. On the other hand, if there are defects in the electroless Ni plating, such as cracks or locally missing Ni plating, this may lead to much faster formation of cracks where the defects are located [160].

Other important factors that may affect the reliability of PTHs are the thickness of the PCB and the hole diameter. A thicker PCB will off course increase the stress on the hole plating, but it may also affect the quality of the hole plating. The thickness of a PCB divided by the diameter of a drilled hole is defined as the aspect ratio for the hole. The higher the aspect ratio, the larger risk for an uneven coating that is thinner in the centre of the hole. Thus, holes with small diameters are generally much more prone to formation of cracks in the hole plating [160]. On the other hand, holes with a large diameter increase the risk for interconnect failures to inner layers.

The reliability of PTH barrels and interconnections to inner layers are also affected indirectly by the material properties of the laminate. The through holes are usually manufactured by mechanical drilling. The drills will wear out with time and if they are not replaced enough frequently, the result will be uneven walls in the holes. This will result in uneven PTH barrel platings with inferior reliability. The increased degree of cross-linking of the resin and the increased levels of fillers in many laminates developed for lead-free soldering increase the hardness of the laminate resulting in faster wear of the drills.

Furthermore, during drilling resin will be smeared on the surfaces of interconnecting conductors in inner layers. Filler particles may also be deposited on exposed conductor surfaces.

Before plating the PTH barrels, the smeared resin and deposited particles must be removed. This is done in a process called desmearing, which is an etching process usually done using a permanganate solution. The increase of the degree of cross-linking in the resin to improve the thermal stability also makes it more chemical stable. Therefore, it may be necessary to adjust the desmearing process to assure good adhesion between the PTH barrel and interconnected conductors in inner layers. This is also the case if laminates with non-halogenated flame retardants are used [161].

### 9.8.2 Pad cratering and copper trace fractures

Pad cratering is defined as "a separation of the pad from the printed board resin/weave composite or within the composite immediately adjacent to the pad [162]. It is called pad craters since it leaves a crater in the laminate if the pad is ripped off. This type of crack is mainly associated with very high strain rates caused by bending, drops, vibration, or fast temperature changes during cool-down in a soldering process [118, 119, 120, 163, 164, 165]. An increase of delta T during thermal cycling has also been shown to increase the likelihood for pad cratering [165].

To a large extent, it is the same factors that affect pad cratering as brittle fractures in solder joints and the conditions that cause brittle fractures may also cause pad cratering. As for brittle fractures in solder joints, pad cratering is mainly a reliability problem for grid array components.

Typical pad cratering cracks are shown in Figure 21 and Figure 23. The pad may be completely or partly separated from the laminate. If via-in-pad is used to connect to the pad, pad cratering can cause a fracture in the connection as shown in the image to the right in Figure 23. If connection to the pad is achieved through a conductor on the top surface, the functionality of the assembly may not have been affected. However, pad cratering often leads to that conductors connected to the pad are fractured (copper trace fracturing) [166, 167]. It also increases the risk for that the pad is ripped off if rework or repair is performed. As for brittle solder joint fractures, a complete pad separation may be the result of one single high-strain event or many consecutive events at a lower strain level.

If laminate cracking occurs in field environments, it may cause other types of failures such as current leakage in the laminate due to ingress of water and contaminants [167] or interconnections failures of conductors connecting to the solder pad.

Several factors may contribute to increased risk for pad cratering in lead-free assemblies compared to SnPb assemblies [168]:

- Pb-free solders are generally stiffer than SnPb solders. Consequently, they can transfer more of the applied global strain to the PCB.
- Phenolic-cured PCB materials typically used in Pb-free assemblies are more brittle than conventional dicy-cured FR-4 materials [169].
- The higher reflow temperatures and cooling rates which Pb-free assemblies are subjected to can lead to higher strains in the assembly. These strains could eventually

relax over time, but if mechanical strain is applied shortly after reflow, pad cratering could occur at lower mechanical strain levels.

- The temperature range from solder solidification to the printed board glass transition temperature is roughly doubled in lead-free soldering compared to for tin-lead soldering. This could lead to a doubling of any thermal expansion mismatch, which could, in turn, increase the propensity for pad cratering.

Laminates filled with inorganic fillers in order to reduce z-axis expansion are more prone to pad cratering in single overstress events [167, 170] whereas non-filled laminates have faster crack growth in cyclic conditions [167]. The cracks in filled resin system tend to form very shallow within the resin layer with no glass weave exposed in the fracture whereas unfilled resin systems will typically fail by fracturing deep through the resin exposing glass fibre bundles [167].

For high $T_g$ dicy-cured materials, multiple reflows will increase the susceptibility for pad cratering whereas high $T_g$ filled phenolic materials are not significantly impacted [169].

The smaller the pad area is, the larger risk for pad cratering. Thus, non-solder mask defined pads are more prone to pad cratering than solder mask defined pads.

The highest 65elecom-mechanical stress that solder joints will be exposed to will occur during the cooling phase after soldering. Hence, it is possible that laminate cracks are initiated in the soldering process. Even very small cracks initiated in the laminate during soldering could possibly change the failure mode from fatigue cracking of the solder joints to laminate cracking [171]. In fact, it has been shown that pre-stress on the laminate prior to a thermal cycling test may cause latent damages in the laminate which cannot be observed as cracks in cross-sections but still increase the risk for laminate cracking in a subsequent thermal cycling test [164].

Soldering processes increase the hardness of PCB laminates due to the exposure to high temperature [163, 172]. A higher hardness probably makes the laminate more brittle and thus more vulnerable to laminate cracking. The increase in hardness is higher in lead-free soldering due to the higher soldering temperature [172]. Since HASL is basically a soldering process, where the PCBs actually are exposed to even higher temperatures than during assembly, HASL can be expected to increase the susceptibility to laminate cracking, especially for lead-free HASL.

### 9.8.3 Formation of conductive anodic filaments

A failure mechanism related to ECM is formation of conductive anodic filaments (CAFs). The main difference is that CAF forms inside PCBs whereas ECM forms on the surface. As for ECM, CAF results in current leakage and, in worst case, short circuits. According to IPC-9691 [173], "*CAF growth is a conductive copper-containing salt created electrochemically that grows from the anode towards the cathode subsurface along the epoxy/glass interface*". It is associated primarily with mechanically drilled holes where the mechanical drilling disrupts the glass reinforcement fibres in glass bundles permitting the absorption of subsequent processing chemistry between the fibres and epoxy (Figure 32). This chemistry is then locked in during plating of the drilled holes.

The growth of CAF may occur between two plated through holes, between a conductor and a plated through-hole, or between two conductors. It may also form in hollow glass fibres [174] or in fractures in the resin.

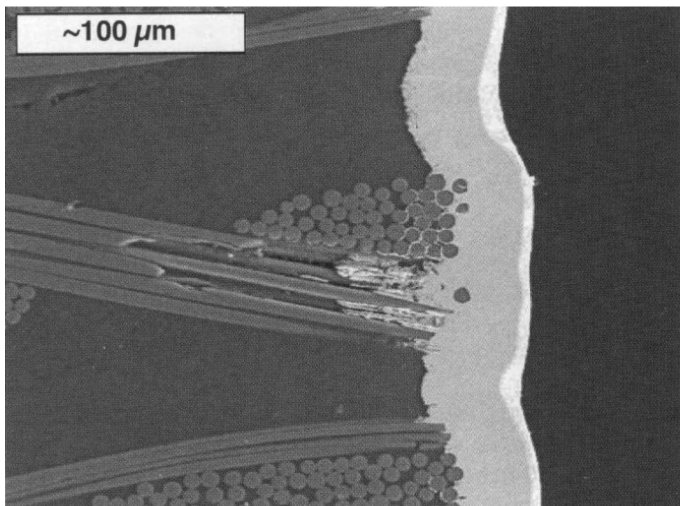



*Figure 32 - Example of a typical disruption of a glass fibre bundle in a plated through hole caused by drilling [173].*

The formation of CAFs consists of complex reactions that are mainly affected by the amount of water present, surface and resin ionic impurities and applied bias [175, 176]. Basically, it is an electrochemical process occurring between two biased conductors with different potential. At the conductor with positive potential (anode), copper ions are formed. These will migrate towards the cathode resulting in the formation of a pathway with increasing conductivity. Most of the copper ions will be precipitated as insoluble compounds somewhere between the anode and the cathode. If the copper ions reach the cathode, they will be reduced to metallic copper and a copper filament will grow back along the pathway towards the anode. The decreasing resistance may itself cause failures but with time may also cause short circuits.

See reference 3 for a more extended discussion of this topic.

### 9.8.4 Formation of whiskers

Tin whiskers are electrically conductive, crystalline structures of tin that sometimes grow from surfaces where tin (especially electroplated tin) is used as a final finish [177]. They generally have the shape of very thin, single filament or hair-like protrusions that emerges outward (z-axis) from a surface. Tin whiskers have been observed to grow to lengths of several millimetres and in rare instances to lengths in excess of 10 mm. Numerous electronic system failures have been attributed to short circuits caused by tin whiskers that bridge closely-spaced circuit elements maintained at different electrical potentials.

Electroplated surfaces with pure tin are most prone to form whiskers. Alloying tin with other elements and especially with lead or bismuth decrease the risk for whisker formation significantly. However, whiskers may still form on SAC solders although the risk is lower [178]. Whiskers may even form on SnPb solders, but they are then normally less than 50 μm long [177].

While the precise mechanism for whisker formation remains unknown, it is known that the following factors can promote whisker growth [177, 178]:

- Residual stresses within the tin plating caused by factors such as the plating chemistry and process. Electroplated finishes (especially bright finishes) appear to be most susceptible to whisker formation because bright tin plating processes can introduce greater residual stresses than other plating processes.

- Intermetallic formation. The diffusion of the substrate material into the tin plating (or vice versa) can lead to formation of intermetallic compounds (such as $Cu_6Sn_5$ for a Sn over Cu system) that alter the lattice spacing in the tin plating. The change in lattice spacing may induce stresses to the tin plating that may be relieved through the formation of tin whiskers.

- Externally applied compressive stresses such as those introduced by torquing of a nut or a screw or clamping against a tin-coated surface can sometimes produce regions of whisker growth.

- Bending or stretching of the surface after plating (such as during lead-formation prior to mounting of an electronic component).

- Scratches or nicks in the plating and/or the substrate material introduced by handling, probing, etc.

- Coefficient of thermal expansion mismatches between plating material and substrate.

- Corrosion of the tin surface.

Since whiskers growth can be affected by so many different types of stresses, there is no simple remedy for preventing formation of whiskers. However, different methods can be used to apply the tin finish and there are also treatments after the application of the finish that can decrease the risk for formation of whiskers. Although, it may be difficult for a designer to influence the type of finish on components, it is important to assure that a whisker resistant finish has been used.

# 10. Reliability assessments

## 10.1 General about reliability assessments

**If a test for assessing reliability shall be adequate**, there must be a clear correlation between the results from such a test and failures occurring in field conditions. Too often, tests are used because they are easy to use, inexpensive and/or give fast results, or just because they have been standardised, without considering whether they are relevant or not. Therefore, it is essential to understand which failure mechanisms may be crucial for a product's reliability in its intended field conditions and how reliability testing should beperformed to be relevant.

Failure mechanisms can be divided into three types depending on the cause of the failure: presence of defect, overstress and wear-out. The type of failure mechanism will affect how the reliability is best assessed. In this document, only failures caused by overstress and wear-out will be covered.

### 10.1.1 Failures caused by overstress

An overstress failure is caused by a single event or a few events that cause the failure. For example, if the intrinsic strength of a material is exceeded in a single event of high stress resulting in a fracture failure, the failure is defined as an overstress failure. Overstress failures can occur both during manufacturing and use. Sometimes an overstress failure may be initiated during soldering or handling of assemblies but not manifested in a failure until in use. An example of a such initiated overstress failure is an initiated brittle fracture in the IMC layer on a solder pad during soldering. Examples of other stresses that may cause overstress failures are:

- Deterioration of material due to exposure to too low or too high temperatures.
- Brittle fractures in solder joints caused by chock, for example due to dropping to the floor.
- Short circuit due to condensation of water.
- Electrical overstress (EOS).
- Electrostatic discharge (ESD).
- Electromagnetic interference (EMI).

### 10.1.2 Failures caused by wear-out

Wear-out failures are caused by accumulation of incremental damages due to exposure to stress or due to aging. Common wear-out failure mechanisms are:

- Fatigue of solder joints.
- Fatigue of platings in trough holes.
- Embrittlement of polymers due to aging.
- Electromigration.

Some failure mechanisms can occur as both overstress and wear-out failures or as a combination of these. For example, electrochemical migration is strongly influenced by the humidity level. If the humidity is kept below a certain level, electrochemical migration will not occur. At humidity levels above the critical level, electrochemical migration takes place faster the higher the humidity level and is best described as a wear-out mechanism. However, if condensation occurs, short circuit due to electrochemical migration may happen within seconds, i.e. a typical overstress failure. Other examples of failure mechanisms that are a combination of wear-out and overstress are various types of corrosion processes.

### 10.1.3 Assessment of failure probability

The probability for failure due to various failure mechanisms can either be assessed from field data or, when that is not available, from reliability tests. If it can be assessed from field data, large costs will be saved, but that is usually only possible to a limited extent, especially when new technology is implemented. The types of tests to perform depend on the type of failure mechanisms. Reliability tests are usually associated with wear-out failure mechanisms and, therefore, tests for wear-out failures will be discussed first.

### 10.1.4 Different types of reliability tests

In a *true reliability test*, i.e. a test that estimates the probability of failure at a given time under given conditions, testing must be continued until enough parts have failed for a life distribution to be determined [179]. This type of test is also called *life test*.

In Annex B to Part 1 of ISO 16750 [36], an example of life test of reliability is given. For determineing reliability, the following step-by-step method is suggested:

*a) Determine the type of load which is relevant for service life and specific to the product and determine the test to be conducted.*

*b) Determine the in-practice load, for example running time, mean temperature, etc.*

*c) Specify the survival probability and confidence levels and calculate the necessary number of DUT or a test duration on the basis of in-practice load, based on statistical correlation. Generally, this calculation requires extensive testing.*

d) *A reduction of this extensive testing resulting from step c) to feasible values can be performed by a permissible increase of load on the basis of an appropriate correlation between in-practice experience and testing. The increase in load shall not lead to a change of the expected damage process. Generally, compared to the check of potential design weaknesses, considerably more extensive testing will be required.*

It is pointed out that "*The method described can be used successfully if there is distinct failure behaviour due to wear or fatigue and if a high increase in load is permissible for testing. This is often applicable to mechanical and electro-mechanical products. Unfortunately, this method can generally* ***not be used for purely electronic components****, because the more accidental failure behaviour (Weibull form factor approximately 1)* ***leads to intolerably extensive testing*** *(number of DUT and test duration) and an increase in load (e.g. temperature rise) is only possible to a moderate extent.*"

Consequently, very few tests in standards for assessing the reliability of PBAs are true reliability tests. An alternative is to run a shorter test and specify a maximum number of failures permissible during a specified test period. For applications where the failure mechanisms and acceleration factors are well known, this type of testing may be sufficient. If the failure mechanisms are not well known and no or few failures occur, it may be difficult to judge the relevance of the test. This latter type of testing is usually called *qualification testing* [180].

However, the most common definition of qualification testing is probably the one given in IPC-T-50 [181]:

*"The demonstration of the ability to meet all of the requirements specified for a product."*

This definition is consistent with the definition of quality in the standards-based approach for reliability assurance. With such a definition of qualification testing, the types of tests could be any of the three types described, i.e. reliability, qualification (in its more restricted meaning) or quality tests (see below), depending on how the requirements have been worded in the specifications.

In many cases, the crucial failure mechanisms are not known well enough for designing a reliability or qualification test. Often in such cases, tests are used that have severe test conditions in order to achieve a high acceleration factor and, thereby, a short duration of the test. In order to save money and/or time, such tests are often preferred instead of reliability or qualification tests, even when such are available. Due to the severe test conditions and the high acceleration factor, irrelevant failure mechanisms may be the dominant causes of eventual failures. It may be adequate when long experience has verified the relevance of the tests, but should always be used with caution. This type of testing is sometimes called "*quality testing*" [179] but is more correctly described as *environmental stress screening – ESS*.

Nevertheless, this type of ESS testing has a value as a tool to detect design weaknesses and manufacturing defects. An example of a design weakness that can be detected is a design with an inappropriate eigenfrequency.

There exist also other definitions of quality, qualification, and reliability testing as well as other terms for these types of testing, for example, integrity testing. Often, a definition of the term used is not given. No wonder that these varying definitions and often inadequate use of the terms in this field cause many misconceptions and misunderstandings.

### 10.1.5 Accelerated reliability testing of wear-out failure mechanisms

For wear-out failure mechanisms, accelerated reliability tests are usually required in order to achieve test results in a reasonable time. Acceleration of a test can be achieved in two ways, which may be combined [180]. The *frequency* of the occurrence that causes failure can be accelerated or the *severity* of the conditions causing the failure can be increased. In general, a failure mechanism that is a continual process going on most of the time, for example a corrosion process, can best be accelerated by increasing the severity of the conditions that cause failures, while a failure mechanism that is caused by a number of sequential events of rather short duration can best be accelerated by increasing the frequency of the events.

Accelerated tests require careful planning if they are to represent the actual usage environment and operating conditions without introducing irrelevant or non-representative failure mechanisms. Failure mechanisms that dominate under normal usage may lose their dominance if the stress levels are increased too much, whereas failure mechanisms that are dormant under normal usage may contribute to failures or even become the dominant failure mechanisms at high stress levels. Obviously, the risk for accelerating wrong failure mechanisms is largest when acceleration is achieved through increasing the severity of the conditions causing the failures. Nevertheless, it can also happen when acceleration is achieved through increasing the frequency of the occurrence that causes failures.

Fatigue of solder joints will be taken as an example of the limitations to accelerate a test by increasing the severity and the frequency of occurrences that cause the fatigue. Acceleration is usually achieved both through increasing the severity (larger temperature range) and the frequency of occurrence (temperature cycles per time unit). Thermal cycling is often performed between -40 ºC and 125 ºC or even between -55 ºC and 125 ºC to achieve a high acceleration factor. However, it is recommended that thermal cycling should not be performed outside the range 0 ºC to 100 ºC unless the products will be exposed to temperatures below 0 ºC and/or above 100 ºC [179]. The reason for this recommendation is that in the temperature region from about -20 ºC to 20 ºC, a primarily stress-driven solder response to applied loads at lower temperatures change to a primarily creep/stress relaxation response at higher temperatures. Thus, the damage mechanism will be different if thermal cycling is performed down to -40 ºC or -55 ºC compared to cycling down to 0 ºC.

Furthermore, if the selected high temperature extreme comes close to $T_g$ (glass transition temperature) of the PCB laminate, this may have a large impact on the failure mechanism [180]. If FR-4 is used, which is the most common board laminate, it may have a $T_g$ of only about 135 °C, but the laminate starts to soften at about 25 ºC lower temperature. That is, a temperature above 110 ºC will cause softening of the laminate which will decrease the stress

applied to the solder joint. Therefore, the high temperature extreme should not be higher than $T_g$ minus 25 °C. However, if the actual product will be exposed to temperatures below 0 ºC and/or above 100 ºC, it is recommended to add a number of cycles similar in nature and number to actual use.

This means that for some applications that are exposed to large temperature changes, for example some under-the-hood applications, the acceleration factor cannot be increased much by increasing the severity, in this case the temperature range. Hence, in such cases, increasing the acceleration factor must be achieved mainly through increasing the frequency of the temperature cycles. A thermal cycle consists of temperature ramps (up and down) and dwell times at the temperature extremes. Therefore, a way to achieve a high acceleration is to make the ramps as fast as possible and the dwell times as short as possible. The most extreme acceleration is achieved if the test vehicle is dipped alternately in two liquids of different temperatures. However, it has been found that this may produce misleading results. Rapid temperature changes cause large transient thermal gradients resulting in warpage of both components and PCB laminate. The warpage will cause both tensile and shear stresses on the solder joints where the tensile loading dominates. Even assemblies with matched CTEs will exhibit solder joint failures when subjected to this type of testing. In contrast, slow thermal cycling results mainly in shear loads and the eventual failure occurs from an interaction of shear fatigue and stress relaxation. Consequently, tests involving rapid temperature changes for purposes of evaluating solder joint reliability are only appropriate if rapid temperature changes at board level are indeed a field condition encountered by the product, which is an unusual condition.

Then remains decreasing the dwell time as a means of decreasing the cycle time. Because fatigue of solder joints is mainly due to creep, a certain dwell time is required to allow for stress relaxation. If the dwell times are too short, the number of cycles required to produce a failure will in fact increase.

This example shows how important it is to have knowledge of the physics-of failure in order to design adequate accelerated tests. All parameters affecting the failure mechanism must be understood and stress levels must be optimised in order to accelerate the relevant failure mechanisms but no non-relevant. Not only operating (testing) parameters affect the test results but also design and manufacturing parameters and these must also be defined. To stay with fatigue of solder joints as an example, the geometry of the solder pads on the component and on the PCB will affect the fatigue life. Thus, reliability testing must also include evaluation and determination of the acceptable ranges of variability (process windows) of these and many other parameters in order to assure the reliability of an end product. Simulation tools can be valuable in the process of identifying the parameters that will be important for various failure mechanisms and for optimising material properties and process parameters. Simulation is normally much faster and less expensive than accelerated tests and can sometimes complement or even replace them.

Failures are in many cases due to a combination of failure mechanisms. *The ideal solution is to find a test that accelerates all failure mechanisms simultaneously in the same manner that will occur during a product's use*, but that is rarely achievable. Tailoring a programme of consecutive tests is usually the only solution. Interactions between various failure mechanisms must

then be considered so that the order of performance of the tests gives the right types of interactions. As an example, vibration may interact with thermal cycling leading to shorter fatigue life of solder joints. In some test chambers, vibration testing can be performed simultaneously with thermal cycling. If such a chamber is not available for testing, a consecutive test must be performed. The order in which the tests are performed can be expected to affect the test results since vibration likely has much more impact on crack propagation than on crack initiation. Therefore, thermal cycling should be performed first but the best solution is to expose the test vehicles alternating to thermal cycling and vibration.

The goal of accelerated tests is to estimate the failure rates of wear-out mechanisms during a product's life. Hence, it must be possible to quantitatively extrapolate from the accelerated conditions to the usage conditions with some reasonable degree of assurance. That is, the acceleration factors for the tests must be determined if they are not already known.

### 10.1.6 Accelerated reliability testing of overstress failure mechanisms

The assessment of the probabilities for overstress failures requires a different strategy. If the failure mechanism is a true overstress mechanism, the goal is to find the stress level at which failures occur. This can be achieved by successively increasing the stress load (step stressing) until a failure is observed. The probability of failure can then be assessed by estimating the likelihood that the determined critical stress level will be exceeded in usage.

In many cases, failure mechanisms are due to a combination of wear-out and overstress, such as electrochemical migration. A combination of accelerated testing and step stressing can then be a useful approach [182].

As for wear-out mechanisms, the design and manufacturing parameters that affect the failure mechanism must be defined and the acceptable ranges of variability of these must be determined. Overstress failures can also be affected by interactions between various types of stresses. Printed board assemblies that may be exposed to condensation of water are usually conformally coated to prevent electrochemical migration. Exposures to low temperatures, fast temperature changes, or vibration may cause cracking of the conformal coating exposing biased surfaces. This may ruin the protection against electrochemical migration. This must be considered when determining the tests to be performed.

Thus, the process of minimising the risk for overstress failure is better described as design-for-robustness than design-for-reliability.

## 10.2 Fatigue life of solder joints

### 10.2.1 Test methods

The fatigue life of solder joints due to cyclic thermomechanical stress is usually evaluated using temperature cycling tests. A number of such test methods are described in IPC-9701, Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments [68].

The important parameters in a temperature cycling test are the temperature extremes, dwell times at temperature extremes, temperature ramp rate and test duration. Five temperature spans are defined in IPC-9701:

- TC1: 0 ºC ↔ 100 ºC
- TC2: -25 ºC ↔ 100 ºC
- TC3: -40 ºC ↔ 125 ºC
- TC4: -55 ºC ↔ 125 ºC
- TC5: -55 ºC ↔ 100 ºC

The fatigue life of a solder joint is to a large degree affected by the extent to which the solder joint is allowed to creep in each temperature cycle. This must be considered when designing accelerated temperature cycling tests. Due to the slower creep rate for lead-free solders, the dwell times for lead-free solders need to be longer than for SnPb solder to reach the same extent of creep in a temperature cycle. In IPC-9701, it is stated that the dwell times should be minimum 10 min for SnPb solder and minimum 30 min for lead-free solders. Maybe it should be even longer for high reliability solders which have a slow creep due to a high degree of precipitation and solid solution hardening (see section 11.3).

The high temperature extreme, $T_{max}$, is also important. As already mentioned, it should not exceed $T_g$ minus 25 ºC. Another factor that needs to be considered when determining $T_{max}$ is coarsening of the IMC precipitates. The degree of precipitation hardening at the start of a thermal cycling test and the rate of coarsening during the test may have a large impact on the fatigue life of the solder joints in the test. Since precipitation hardening is affected by the volume of solder joints, the degree of precipitation hardening may differ a lot for various components on the same assembly.

A high degree of precipitation hardening may delay the recrystallisation in a test with low $T_{max}$ resulting in a long fatigue life. However, the higher the $T_{max}$ in the test, the faster will the coarsening occur. Thus, for solder joints with low degree of precipitation hardening, a high $T_{max}$ will have a low impact on the fatigue life whereas it may have a large impact on solder joints with high degree of precipitation hardening. As a consequence, the acceleration factor may be different for various components on an assembly in the same test and the difference may be very large.

Shirazi et al. [183] evaluated the fatigue life of four model CSP packages with varying pitch, solder volume and pad size using two thermal cycling tests. In one of the tests, the test vehicles were cycled between -40 °C and 125 °C and in the other test they were cycled between 0 °C and 80 °C. Figure 33 shows the results from the two tests. The solder volume for the packages increases from Package A to Package D. That is, package A has most precipitation hardening. Whereas package A performed rather poor when tested between -40 °C and 125 °C, it outperformed the other packages when tested between 0 °C and 80 °C. If the acceleration factor

is calculated as the ratio between the characteristic lives in the milder test and that in the harsher test, it was 14, 8.5, 5.3 and 4.5 for packages A, B, C and D, respectively.

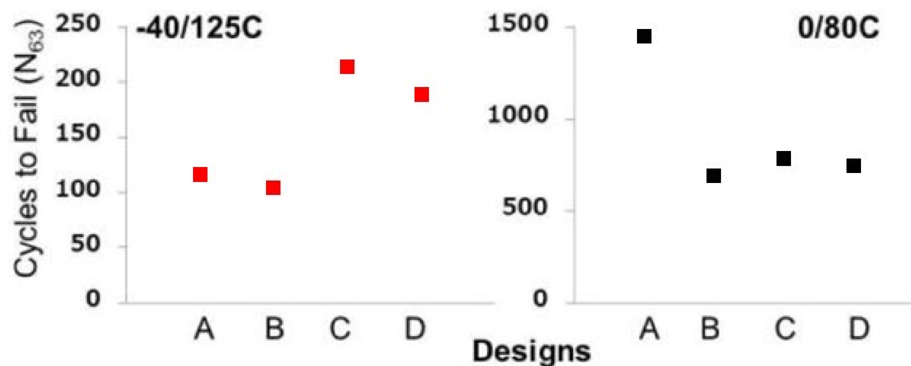



*Figure 33 - Characteristic number of cycles to failure for four area array designs with varying solder joint volume in -40/125 ºC cycling (left) and 0/80 ºC cycling (right). A denotes smallest volume and D denotes largest volume [183].*

This means that a too high $T_{max}$ in a thermal cycling test may lead to a large underestimation of the fatigue life in field conditions for packages with a high level of precipita-tion hardening.

The test should be continued to whichever condition occurs first:

- 50 % or preferred 63.2 % of cumulative failure.
- 6 000 cycles for TC1 (preferred reference thermal cycle).
- 1 000 cycles for TC2, TC3 and TC4.

The preferred temperature cycle is TC1. For assemblies seeing significant cold environment operations (below 0 ºC), IPC-SM-785 recommend adding cold cycling, from perhaps -40 ºC to 0 ºC, for a number of cycles equal to the cold ºC operational cycles in actual use [179]. Similarly, for products seeing large cyclic temperature swings, additional appropriate large delta-T testing with cycles similar in nature and number to actual use is recommended.

According to IPC9701, the temperature rate ramp should be maximum 20 ºC/min. Usually, a temperature rate ramp of 5-10 ºC/min is used. If the temperature rate ramp is larger than 30 ºC/min, it is defined as a temperature shock test [179]. It may cause temperature gradients in the test object that might affect the failure mechanisms in a way that would not occur in field conditions. Therefore, it should be avoided unless such fast temperature changes may occur in field conditions.

In thermal cycling tests, components and PCB will have approximately the same temperature. However, for many products, heating is due to power dissipation. This will result in large temperature gradients inside packages, between packages and PCB, and within the PCB. This is a rather different situation compared to thermal cycling. Even if all materials have matched CTEs, power dissipation may cause fatigue. It has been shown that power cycling and thermal cycling show significant differences in failure location [184]. Therefore, thermal cycling may

give misleading results if heating is due to power dissipation. In such cases, power cycling is more appropriate [76, 185]. Maybe, a thermal shock test could be an alternative.

Since aging prior to thermal cycling will cause coarsening of the IMC precipitates, it will result in smaller $N_{coars}$ and thus faster fatigue failures. Even storing at room temperature may have this effect. Six months of storing at room temperature may cause an up to 100 times increase in steady state creep strain rate [186]. Generally, the higher the aging temperature and the longer the aging time, the larger decrease of $N_{coars}$ [76, 185]. After aging at 50 °C for 50 hours, the creep resistance of SAC alloys may even become lower than that of SnPb.

Since it will take some time before most products will be used after production, preconditioning prior to thermal cycling in order to achieve some coarsening of IMC precipitates may improve the relevance of the test. This may be even more important in the case of products that are exposed to high temperature for a long time in each cycle in the field. A significant coarsening can then be expected during rather few cycles. IPC-9701 does not specify any requirements regarding preconditioning prior to thermal cycling but mentions that "*Select non-commercial customers prefer that test vehicles, following board assembly, should be subjected to an accelerated thermal aging (e.g., 24 hours at 100 °C) in air to simulate a reasonable use period and to accelerate such possible processes as solder grain growth, intermetallic compound growth, and oxidation. Storing the test vehicles after this artificial aging for some additional time at room temperature before commencing with the fatigue serves to further stabilize the solder structure*".

### 10.2.2 Test vehicles

If it shall be possible to correlate the results from a thermal cycling test to field performance, the test vehicle needs to be representative for the actual product. Ideally, testing of a functional product would give that information but they are not suitable for assessing the fatigue life of solder joints since it is difficult to determine when failures occur for a specific component.

Thus, it is necessary to use specially designed test boards that facilitate monitoring of the electric continuity of all solder joints to each specific component. Proper design and assembly of the test vehicles are critical to assure that valid and appropriate data are obtained [68]. Both the PCB and the components as well as assembly processes need to be representative for true products. Furthermore, the semi-conductor components must have internal chips and daisy-chain interconnections to facilitate continuous monitoring of the integrity of all solder joints during testing. These are mandatory requirements in IPC-9701.

### 10.2.3 Acceptance criteria

Although the title of IPC-9701 is "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments", it does not contain any acceptance requirements. Instead, it is stated in the standard that "*At this point in time, the reliability requirements need to be established by agreement between customer and supplier*".

However, IPC-9701 defines a number of product categories and worst-case use environments for these [68]. Three of the categories are "Telecomm", "Industrial and automotive – passenger compartment", and "Military (ground and shipboard)". All three are assumed to be exposed to 365 thermal cycles/year.

For the 76elecom category, all of the cycles are assumed to have a ΔT of 35 ºC. The expected service life is 7-20 years with an accepted failure risk of 0.01 %.

For the industry/automotive compartment category, 50 % of the cycles are assumed to have a ΔT of 20 ºC, 27 % a ΔT of 40 ºC, 16 % a ΔT of 60 ºC and 6 % a ΔT of 80 ºC. The expected service life is 10-15 years with an accepted failure risk of 0.1 %.

For the military category, 27 % of the cycles are assumed to have a ΔT of 40 ºC and 73 % a ΔT of 60 ºC. The expected service life is 10-20 years with an accepted failure risk of 0.1 %.

According to Willems et al. [114], the number of cycles to 63 % failures (eta) in a thermal cycling test between -40 ºC and 125 ºC needs to be:

- >1 000 cycles for 7 years lifetime and >3 000 cycles for 20 years lifetime for the 76elecom category.
- >1 500 cycles for 10 years lifetime and >2 250 cycles for 15 years lifetime for the industry/automotive compartment category.
- >2 750 cycles for 10 years lifetime and >5 500 cycles for 20 years lifetime for the military category.

If thermal cycling instead is performed between 0 ºC and 100 ºC, the required number of cycles to 63 % failures doubles for all categories.

Examples of acceptance criteria used by companies can be found in the literature, but almost exclusively for automotive electronics. According to Mawer et al. [79], typical requirements for under-hood applications where in the nineties:

- Failure free after 1000 cycles -40 ºC to 125 ºC with an 1.5 hour cycle.
- Failure free after 2000 cycles -40 ºC to 125 ºC with an 1 hour cycle.
- The number of cycles to 1 % failures $N_1$ should be more than 2500 cycles when cycled between -40 ºC and 125 ºC with an 1 hour cycle.

In 2014, it was common to require 3 000 cycles without failure for under-hood applications when cycled between -40 ºC and 125 ºC (cycle time not specified), according to Carpenter et al. [189].

In 2021, Ribas et al. [190], specified the required numbers of cycles in various thermal cycle tests for automotive electronics as shown in Table 9.

Table 9 - *Typical number of cycles requirements for automotive electronics [190].*

| Temperature cycle | Powertrain | Body | ADAS* | Chassis & safety | Infotainment |
|---|---|---|---|---|---|
| -40 °C / 150 °C | 2 000+ | | 2 000+ | 2 000+ | |
| -40 °C / 125°C | | 2 000+ | 2 500+ | 2 500+ | 1 000+ |
| -40 °C / 105 °C | | | | | 1 500+ |

** Advanced driver assistance systems*

However, in none of these examples was it specified what the acceptance requirements for automotive electronics were based on.

Together with SAE (Society of Automobile Engineers), ZVEI (German Electrical and Electronic Manufacturers' Association) has produced handbooks on how to validate the reliability of automotive electrical and electronic modules [191] and of semiconductor components in automotive applications [192]. Several of the largest vehicle manufacturers and their subcontractors were involved in the development of the two handbooks and JSAE (Japanese Society of Automotive Engineers) contributed also to the development of the latter handbook.

According to the automotive module handbook, it has been practice to ensure reliability with a "*test to pass*" test where 6-24 units have been tested with zero fault requirements. However, with this type of test, it is not possible to verify failure levels lower than 1 000 ppm. It would require testing of thousands of devices.

If no failures occur during testing, it means that:

- Actual reliability is not known.
- The acceleration factor for the test is not measured.
- The intended failure mechanism has not been verified.
- The dominant fault mechanism may not have been sufficiently accelerated to verify that the service life requirements have been met.

Therefore, to verify low failure levels, one must test to "*end of life*", or at least until so many units have failed that one can determine the expected failure outcome as a function of time. This means that you qualify for "*fit for use*" and not "*fit for standard*". The reason for testing to failure is also to get an idea of what safety margin you have.

Qualification of components performed by component manufacturers according to AEC-Q100/101 does not normally include testing solder joint fatigue life of soldered

components. According to the handbook for the validation of semiconductor components, this should therefore be done in addition to the tests in the AEC-Q100. Furthermore, if there is a developed acceleration model for a failure mechanism, it can be used to calculate the number of cycles you need to perform *without failure* to verify sufficient reliability. An example for 2nd level solder joint fatigue is given as shown in Table 10.

Table 10 - *Number of cycles required for assuring 2nd solder joint fatigue reliability according to ZVEI Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications [192].*

| Loading | Mission Profile Input | Stress Conditions | Critical failure mechanism | Acceleration Model (all temperatures in K) | Model Parameters | Calculated Test Duration |
|---|---|---|---|---|---|---|
| **Thermo-mechanical** | $n_u$ = 11,000 cls number of cold starts over 15 years of use)<br><br>$\Delta T_u$ = 80 °C (average thermal cycle temperature change in use environment) | $\Delta T_t$ =165 °C (thermal cycle temperature change in test environment: -40 °C to 125 °C), Test: TC | 2nd level (board level) solder joint fatigue | Norris-Landzberg<br>$A_f = \left(\frac{\Delta T_t}{\Delta T_u}\right)^a \left(\frac{t_t}{t_u}\right)^b \exp\left[c\left(\frac{1}{T_{max,u}} - \frac{1}{T_{max,s}}\right)\right]$<br><br>Modification according to Pan N. et al, Proc. SMTA, 2005 | a = 2.65<br>b = 0.136<br>c = 2185 | $n_t$ = 865 cycles (number of cycles in test)<br><br>$n_t = \frac{n_u}{A_f}$ |

That is, in this case it is, of some reason, apparently not considered necessary to test until enough many units have failed that you can determine the expected failure rate as a function of time. It may be relevant if you are absolutely sure that the acceleration model is correct. However, if you read the article referred to in the table [193], it will turn out that the acceleration model is calculated from testing three component types: a ceramic BGA with 2 533 I/Os, a centre wire-bonded CSP with 60 I/Os and a TSOP with 56 I/Os and alloy-42 lead frame. None of these three component types are normally found in automotive electronics. When thermal cycling the CSP component between -25 and 125 °C, it had a characteristic life of only 167 cycles and a beta value of 2.93, i.e. it would far from meet the requirement of 865 cycles when cycling between -40 °C and 125 °C, which neither the ceramic BGA would have done. Furthermore, the article states that the acceleration model is uncertain at temperatures below 0 °C and above 100 °C and readers are recommended to use a safety factor when using the model to predict field life. None of this is mentioned in the ZWEI manual.

There are clearly no generally accepted or even less specified criteria in standards for accelerated thermal cycling tests, and perhaps there should not be any. As described before, the goal of accelerated tests is to estimate the failure rates of wear-out mechanisms during a product's life. If that shall be possible, it must be possible to quantitatively extrapolate from the accelerated conditions to usage conditions. That is, the acceleration factors for the tests must be determined.

As described, the failure mechanism may change if the maximum temperature in a thermal cycling test is increased to temperatures above 100 °C, especially for lead-free solder joints. The coarsening of IMC particles will get faster that might lead to an underestimation of the fatigue life, and cracks may form in the PCB and BGA substrates that might lead to an over-estimation of the fatigue life.

Therefore, because many products experience temperatures close to 100 °C, or some even higher temperatures, acceleration of thermal cycling tests can mainly be achieved by increasing the frequency of the cycles. However, the cycle time needs to be at least 1 hour, so the frequency cannot be increased very much either. Since many products have an expected field life of 10 to 20 years, it would require very long tests to determine the acceleration factor for a thermal cycling test.

Even if that is performed, the test conditions would in most cases differ considerably from field conditions. In field conditions, the temperature will in most cases fluctuate, that is you would have a number of superimposed smaller temperature cycles that also will affect the fatigue life. Furthermore, heating of assemblies is often caused by power dissipation. This may result in large temperature gradients inside packages and between packages and PCB. That might result in different stress conditions for the solder joints compared to thermal cycling tests.

Many products will also be exposed to vibration or even shock during use which might also affect the fatigue life of the solder joints. Rather little work has been done on how vibration affects the fatigue life of solder joints. Even less studies have been performed of the impact of combined thermal cycling and vibration/shock. When thermal cycling and vibration is performed, they are usually performed as consecutive tests assuming linear damage accumulation (Palmgren-Miner rule). That is, the result of testing is assumed to be the same independent in which order the tests are performed.

However, there are a number of studies indicating that this may not be the case for lead-free soldering. Perkins and Sitaraman compared how the order of thermal cycling and room temperature vibration affected the fatigue life of solder joints to ceramic column grid array components [194]. Thermal cycling followed by vibration was a harsher sequence than vibration followed by thermal cycling. The difference was attributed to the severe deformation and microstructural changes that occur in thermal cycling which initiate cracks quickly and accelerate the subsequent crack growth during vibration loading.

Furthermore, according to Yang et al., loading sequences starting with milder cycling and ending with harsher cycling underestimates life while harsh-mild sequences overestimates life [195]. In one experiment, the life was overestimated by more than one order of magnitude. Furthermore, the impact of vibration can be expected to be quite different at high temperatures compared to room temperature.

Automotive electronics are normally exposed to several stresses simultaneously and not sequentially. There are not many investigations comparing the results of combined testing with sequential testing. One such test is an investigation performed by Qi et al., in which the result of combined thermal cycling and random vibration was compared with the result of sequential loading of thermal cycling and vibration using Palmgren-Miner rule [196]. They found that the fatigue life in the combined test was only half of that predicted by Palmgren-Miner rule.

Due to these differences in test conditions and field conditions, it is difficult to set up relevant acceptance criteria for thermal cycling tests. Therefore, a thermal cycling test should be viewed as a qualification test rather than a true reliability test. It will show, for example, how different

materials and components will perform in relation to each other. That is, if you want to implement new technology, for example a new component or a new solder, you should evaluate it together with technology in use that you know is reliable. It will then, hopefully, show you if the new technology will perform better, as good as, or worse than the technology in use. Although, there is no guarantee for that. The new technology could cause changed or new failure mechanisms that affect the results.

## 10.3 Brittle fractures of solder joints

According to IPC-7095A, interfacial fracture happens on nickel surfaces under high levels of both applied strain and strain rate [34]. Nevertheless, the brittleness of solder joints is usually evaluated using shear and pull tests with low strain rate [197, 198, 199, 200, 201, 202, 203]. A few investigations have been performed where the results from tests with high strain and strain rate have been compared with results from traditional shear and/or pull tests [204, 205, 206, 207, 208, 209, 210]. They have all shown that especially traditional shear tests but also pull tests are not adequate for testing the risk for brittle fractures.

Besides shear and pull tests, drop tests are often performed in order to evaluate the risk for brittle fractures. How the drop test is performed may have a large impact on the result. JEDEC has developed a standard for drop testing of components for handheld electronic products, JESD22-B111 [211]. For portable products, dropping it to the ground usually results in board bending, which is more likely to cause brittle fractures than shock. If a product with the assembly fixed in the corners is dropped with the assembly in a horizontal position, the interconnection stress due to board bending is two orders of magnitude higher than that due to acceleration according to Wong et al. [207]. For that reason, the JEDEC standard requires that the test board be mounted on a base plate with the components facing down. The board shall be fixed to the base plate in the four corners using 10 mm long standoffs to allow bending of the board. The base plate with the assembly is then dropped with the assembly in a horizontal position.

It is stressed in the JEDEC standard that it is not meant to address and simulate shipping and handling related shock of electronic subassemblies. These are addressed in JESD22-B110 [212]. According to this latter standard, subassemblies may be tested either in the free state or in a mounted state. If the mounted state is performed, the method of mounting to connecting member should be typical of production method. When tested in free state, shock should be applied to the assembly body in a manner to simulate expected impacts during processing, packaging, and packaged shipment. When testing in mounted state, shock should be applied to the connecting member upon which the subassembly has been mounted, using test fixturing in a manner such that the subassembly experiences the full specified test level. During the test, the connecting member should support the printed board of the assembly in a manner which best simulates usage condition of the subassembly, typically allowing the subassembly to flex during the shock test.

IPC and JEDEC have developed a joint standard for characterising the fracture strength of a component’s board-level interconnects when exposed to monotonic bending [213]. The monotonic bend characterisation results provide a measure of fracture resistance to flexural

loading that may occur during conventional non-cyclic board assembly and test operation, and supplements existing standards that address mechanical shock or impact during shipping, handling, or field operation. The test board material, thickness, metal layer count, surface finish, and land pad design should match the actual end-use printed board. A four-point bend test is used to characterise the fracture strength. Since storage conditions and storage duration affects the fracture resistance, it is required that testing is performed minimum eight hours and maximum 168 hours after soldering. According to Bansal et al., components tested within an hour after soldering have lower brittle fracture strength compared to components tested a few weeks after soldering [134]. Therefore, waiting too long before testing may lead to an underestimate of the risk for brittle fractures during handling directly after soldering.

In another standard developed by IPC and JEDEC, guidelines are given for how to perform strain gage testing in order to assess the strain and strain rates a surface mount package is subjected to during PCB assembly, test and operation [133, 214]. It is stated in the standard that "*Many board assemblers are now required to operate under strain levels specified by their customers or component suppliers*". "*PWB strain measurement includes application of strain gages to the board at specified components, and then subjecting the instrumented board to various test and assembly operations. Test and assembly steps which exceed strain limits are deemed excessive and are identified so that corrective actions can be made. Strain limits may come from the customer, component supplier or internal best known practices*". Examples of strain measurement criteria are given in an appendix. Manufacturing steps that can cause strain-induced failures and therefore may need to be characterised include:

1) SMT assembly process: board depanelisation, all manual handling processes, all rework and retouch processes, and connector and component installation.

2) Board test processes: In-circuit test and board functional test.

3) Mechanical assembly: heat sink assembly, board support/stiffener assembly, system board integration, Peripheral Component Interconnect or daughter card installation and Dual in-line memory module installation.

4) Shipping environment.

The strain is measured on the PCB near the components, preferably as close as possible to all corners of a component, either on the top or underside of the board [136]. While the strain within the solder joint cannot be directly measured, results do correlate with data on brittle fractures. In order to test the ultimate strain-to-failure of a component, a board is tested at increasing strain levels until electrical failure is detected [215].

Brittle fractures can occur also during thermal cycling and vibration but there are no standards for how to evaluate that. Mattila and Kivilahti have shown that the number of drops to failure may decrease significantly if the solder joints are aged at 125 ºC prior to drop testing whereas thermal cycling may increase the number of drops [215]. Thus, aging effects must be considered when assessing the risk for brittle fracturing. This is especially important for brittle fracturing caused by formation of microvoids in IMC layers to copper surfaces.

See reference 66 for a more extended discussion of how to test the risk for brittle fractures in solder joints.

## 10.4 Electrochemical migration

### 10.4.1 Test methods

Since electrochemical migration can cause failures within seconds if condensation of water occurs on an assembly, it is practically impossible to design a test that will predict the life of a product due to ECM. What you can design is tests that show the propensity to form ECM during different field conditions.

#### Non-condensing conditions

In conditions where condensation of water will not occur and the assemblies will not be contaminated with dust or other foreign materials, the propensity to form ECM will mainly be affected by contamination present on the assembly after production, and by relative humidity and temperature in field conditions. Since contamination present on an assembly is a crucial factor, and then especially ionic contamination, measurement of the amount of ionic contamination was for a long time the most used method to verify adequate cleanliness of assemblies. The most used method is called resistivity of solvent extract (ROSE) and has been used to verify cleanliness both of PCBs and assemblies. It has been known for a long time that the method has very low measurement accuracy, and the relation between the measured value and field performance is very poor [3, 182, 217]. Therefore, it is stated in IPC-5703 [24] that "*the use of ROSE for product acceptance is not a valid practice, even though it is commonly done in the industry*". Furthermore, in the latest version of IPC J-STD-001, version H, ROSE testing is no longer considered an acceptable basis for qualifying a manufacturing process of assemblies.

Instead of measuring the amount of contamination on assemblies, it is more relevant to measure how contaminants affect the surface insulation resistance (SIR), which is related to the failure mechanism. Surface insulation resistance is defined in IPC-9201 [218] as "*a property of the material and electrode system. It represents the electrical resistance between two electrical conductors separated by some dielectric material(s). This property is loosely based on the concept of sheet resistance, but also contains element of bulk conductivity, leakage through electrolytic contaminants, multiple dielectric and metallisation materials and air*".

That is, SIR is defined as a materials system property. A certain level of SIR is required for the proper function of an assembly, but that is something else than assessing the risk for ECM.

If you start to measure SIR between two conductors, ions between the conductors will start to migrate leading to a depletion of ions between the conductors. At the same time, metal ions

will form at the anode and migrate towards the cathode that will increase the amount of ions between the conductors. That is, SIR will change when you start to measure it. The measured value and how it changes with time can be used to assess the propensity for forming ECM although it is not straightforward how to interpretate the results [182, 217].

Measurement of SIR is performed under controlled temperature and relative humidity. A large number of tests exists for SIR measurements of which some are listed in Table 11.

Table 11 - *SIR tests and test conditions specified for IPC Test Methods 2.6.3 [219] and 2.6.3.3 [220], IEC Test 5E02 [221] and IPC-9202 [31].*

| | IPC Test 2.6.3.3 | IPC Test 2.6.3, Class 3 | IEC Test 5E02 | IPC-9202 |
|---|---|---|---|---|
| Temperature/RH | 85°C/85 % RH | 20 cycles 25-65°C/85-93 % RH | 40°C/93 % RH[1] or 85°C/85 % RH | 40°C/93 % RH |
| Duration | 168 hours | 160 hours | Minimum 168 hours | Minimum 168 hours |
| Bias | 45-50 V DC | 100 V DC | 5, 50 or 100 V DC[2] | 5 V DC |
| Test voltage | 100 V DC with reversed polarity | Optional[3] but with the same polarity as the bias voltage | 5 or 100 V DC[2] with the same polarity as bias | 5 V DC with the same polarity as bias |
| Measurement frequency | After 24, 96 and 168 hours | Every third cycle | Depends on bias and test voltage[2] | At least once every 20 minutes |

*1 No-clean processes shall be tested at 40 °C and 93 % RH.*

*2 Three test conditions are suggested with the following bias/test voltage/test frequency: 50V/100V/24-96-168 hours, 100V/100V/twice daily, and 5V/5V/every 20 min.*

*3 To be specified in procurement documentation.*

As described in section 0, version H of IPC J-STD-001 requires that manufacturers of class 2 and 3 products shall qualify soldering and/or cleaning processes that result in acceptable levels of flux and other residues. One proposed method to do that is to evaluate material and process compatibility per IPC-9202. The standard requires that an SIR test is performed for the material and process characterisation/qualification. The test conditions specified in IPC-9202 are listed in Table 11. It is basically the same test conditions as in IEC test 5E02, but with some modifications.

## Condensing conditions

If a product will be used in field conditions where condensation may occur on assemblies, or dust and other foreign material will be deposited on them, ECM may occur even if the assemblies are extremely clean after production. If a product will be used in such conditions, it will be necessary to protect the assemblies in some way. One possibility is to use a hermetic casing. Another possibility is to conformally coat the assemblies.

If a conformal coating is used, test methods for evaluating the propensity for ECM must then be designed to evaluate the environmental protection provided by the coating. Running an SIR test under non-condensing conditions will only show if the assemblies had adequate cleanliness prior to the application of the conformal coating, or if the coating itself contribute to low SIR. In fact, if the assemblies had high cleanliness prior to the application of the conformal coating, the coated boards normally would show lower SIR values than non-coated boards because the coating material itself provide a medium for current leakage. That is, the test conditions need to be at least as harsh as the field conditions where the product will be used.

Today, no standardised test methods exist for evaluating the environmental protection provided by conformal coatings. Therefore, three test methods, of which two are new, for evaluating the environmental protection provided by conformal coatings have been designed and evaluated in research projects performed at RISE. The three test methods were:

- Mixed flowing gas (MFG) test.
- Salt fog/mist exposure.
- Simulated condensation.

The MFG test did not turn out to be a useful test for this purpose and will therefore not be described here, but it is described in section 11.1.1.

### Salt fog/mist exposure

Two different procedures were used for contaminating the assemblies with salt. In the first procedure, the test boards were placed unbiased in a salt spray test cabinet, and they were then exposed to a fog made of 5 % NaCl dissolved in water at 35 °C per ISO 9227 [222]. In the second procedure, the boards were contaminated with salt by spraying them with a mist of 5 % NaCl dissolved in water using a spray bottle. In both procedures, the boards were allowed to dry after having been contaminated with the salt solution. The boards were then tested with an ECM test using the test conditions specified in IPC-9102. This test method proved to be very decisive for evaluating the environmental protection that a conformal coating provides.

### Simulated condensation

In the simulated condensation test, the test boards were laid in a horizontal position at the bottom of a humidity cabinet, six at a time, as shown in Figure 34.

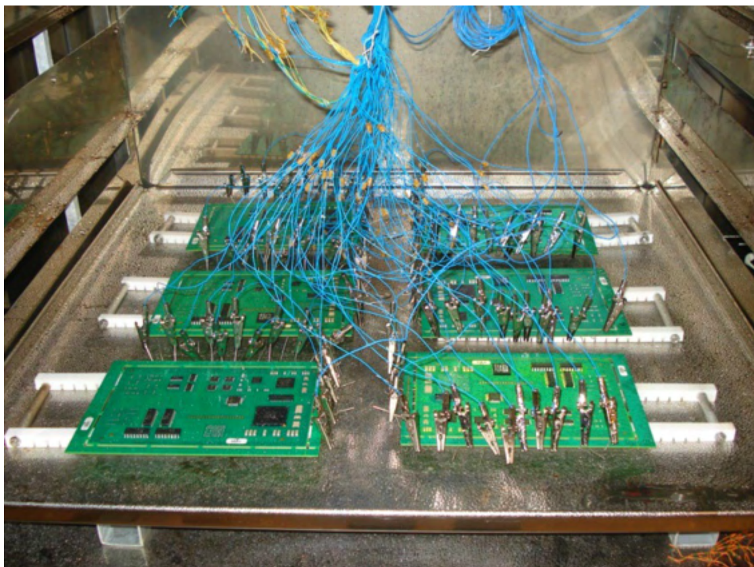


*Figure 34 - Position of the test board in the humidity cabinet during the simulated condensation test.*

A mist of fine water droplets, created by a humidifier, was then let in at the top of the closed cabinet through a tube as shown in Figure 35. The inlet of mist was done at room temperature. This was done for either 10 minutes or 90 minutes. When exposed for themist for 10 minutes,

the amount of deposited water was determined to be 2.2 μg/cm[2] corresponding to a 22 μm thick layer of water. When exposed to the mist for 90 minutes, large droplets of water were formed on the boards as shown in Figure 36.

A bias voltage of 5 V DC was applied to the test patterns during the inlet of the mist and for an additional 20 minutes when the inlet of mist was interrupted after 10 minutes. The SIR for the test patterns was measured using a measurement voltage of 5 V DC with the same polarity as the bias voltage. This test method proved also to be very decisive for evaluating the environmental protection provided by a conformal.

*Figure 35 - Photographs showing the tube used for distributing the mist inside the humidity cabinet.*

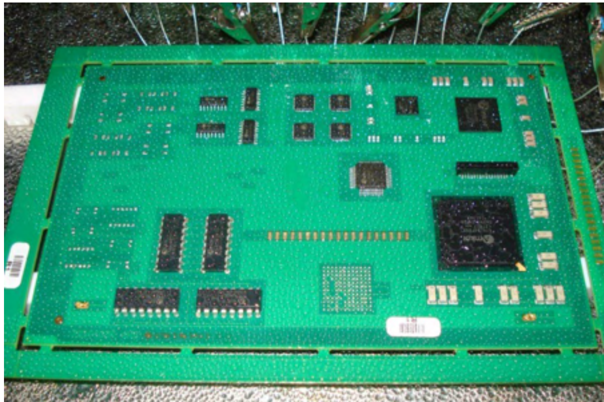


*Figure 36 - Deposited water droplets on a test board after 90 minutes exposure to the mist from the humidifier.*

### 10.4.2 Test vehicles

Originally, test boards with interdigitated comb and/or Y patterns were used for SIR measurements as shown in Figure 37.

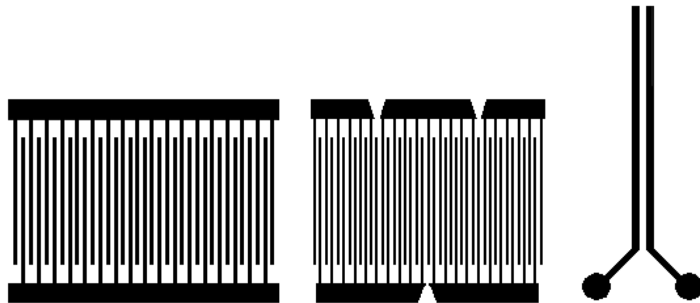


*Figure 37 - Examples of comb patterns and a Y-pattern from Test Board IPC-B-25A used for SIR and electrochemical migration testing.*

Today, many test boards used for SIR and ECM testing have test patterns for components with interdigitated solder lands to obtain test patterns that are more representative of the circuits on assemblies. Thereby, components can be soldered to the test boards to better represent true assemblies. Three examples of such patterns are shown in Figure 38. The two first types of test patterns have also comb patterns beneath the component bodies. These types of test patterns make it possible to mount and solder components to the test patterns. That is, test boards can be produced that go through the same manufacturing and cleaning processes as true assemblies.

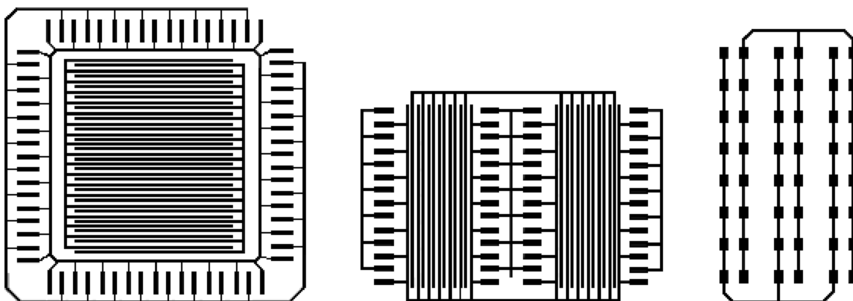


*Figure 38 - Test patterns for measuring SIR between solder joints to an LCCC68 or PLCC68 component, two SO28 components, and 0805 chip capacitors. Comb patterns are located beneath the IC components.*

An example of a modern test board that can be used for SIR measurement of an assembled board is shown in Figure 39. Surface insulation resistance can be measured between solder joints to the various types of components but also for comb patterns located beneath some components. This test board, IPC-B-52, is proposed to be used in IPC-9202, but it is not required to use this test board. Any test board with similar circuitry can be used.

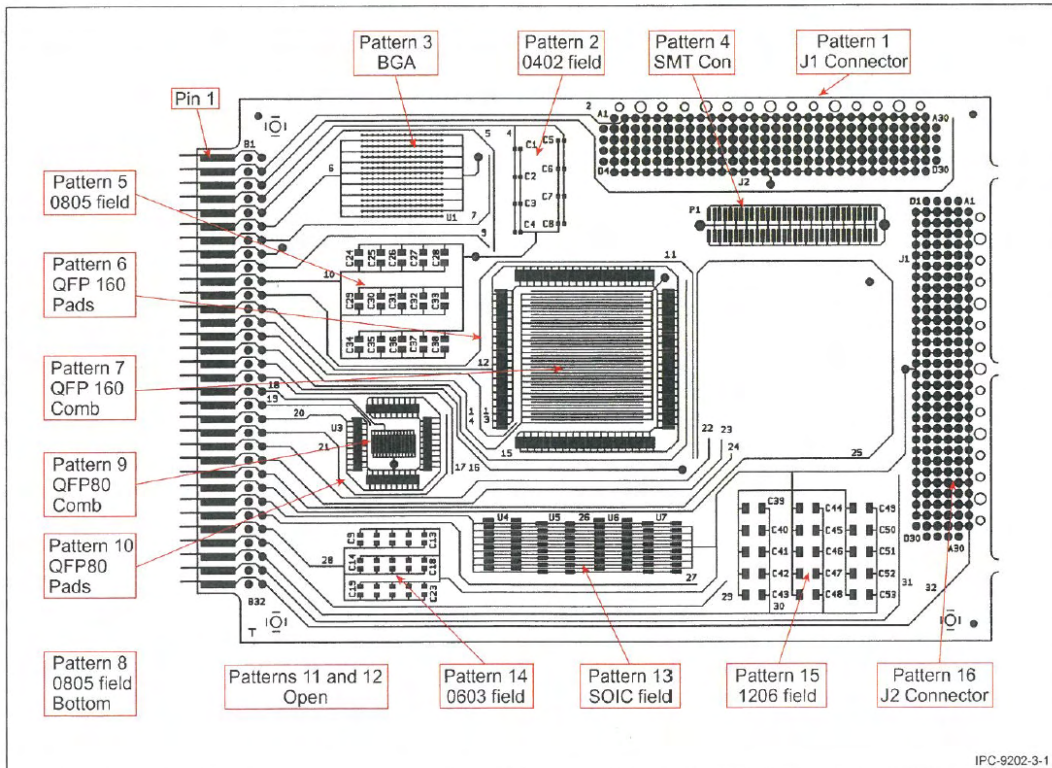



*Figure 39 - Design of test board IPC-B52 for SIR measurements.*

### 10.4.3 Acceptance criteria

The acceptance criteria for ECM in IPC-9202 are:

- All tested SIR patterns shall show a minimum resistance of 100 megohms, beginning 24 hours after the chamber has stabilised at the test conditions.
- Any patterns that exhibit dendrites that extend more than 20 % of the conductor spacing shall be considered failures.

The reason for setting the acceptance criterion to 100 Mohm in IPC-9202 is not given. No investigations have been performed that show that ECM can be prevented if the SIR is above 100 Mohm. When looking in older IPC standards, it can be noted that acceptance criteria for SIR tests usually are chosen in the range of 100-500 Mohm, although the test conditions and the test patterns have varied considerably. In an IPC technical paper from 1985 [223] it is mentioned that the practice at that time was to require an SIR of 100 Mohm, but then only as a requirement for initial resistance. Chan has shown that SIR may increase several decades on a contaminated board during a test period of 100 hours and approach the value of a clean board [224]. Therefore, it seems logical to have a requirement for the initial SIR during a test.

When testing according to IPC-9202, all tested SIR patterns shall show a minimum resistance of 100 Mohm beginning 24 hours after the chamber has stabilised at the test conditions. Since no information is given on the background to this SIR requirement, it is not possible to draw any conclusion about the relevance of the requirement, or to justify the disregarding of initial SIR values. It is also a bit odd that the SIR requirement is the same for all test patterns independent of the sizes of the test patterns and the insulation distances between the biased surfaces. Both the size of a test pattern and the insulation distance between biased surfaces will of course affect SIR.

If extensive ECM occurs, it may cause a drop of SIR during the test to values below 100 Mohm, but not always. If a dendrite crosses the distance between the electrodes, it will cause a short circuit that burns off a part of the dendrite. That is, it will cause a drop in SIR, but this drop in SIR is so short that it is normally not registered. After a part of the dendrite has been burned off, the SIR is restored. That is, dendrites may form without any change of SIR values. Therefore, it is required to visually examine the test patterns after the test to judge whether dendrites have formed during the test.

As for thermal cycling tests to assess fatigue life of solder joints, ECM tests should be viewed as qualification tests, and not true reliability tests. They are useful tests for evaluating how a change of material(s) or process(es) affect reliability compared to material(s)/process(es) already in use. Passing the requirement of 100 Mohm is no guarantee for that ECM will not occur in field conditions, but it can be used as a baseline for verifying adequate cleanliness after assembly. It can be noted that IEC standard 61189-5 [221] does not contain any acceptance criteria at all. It only specifies how the test should be performed, how it should be evaluated and what the test report should contain.

Traditional ECM tests of conformally coated boards will only show if the assemblies were adequately clean prior to the application of the coatings or if the coatings themselves will contribute to low SIR values. They will not show if the coatings will provide environmental protection in harsh conditions. To verify that, more severe test conditions are required, for example exposure to salt solution or simulated condensation of water. Such tests can be useful to discriminate the capability of the various conformal coatings to provide protection in harsh conditions.

## 10.5 CAF

### 10.5.1 Test method and test vehicles

IPC has defined a test method for testing the propensity for forming CAF including design of test vehicles, Test Method 2.6.25A, Conductive Anodic Filament (CAF) Resistance Test: X-Y Axis [225]. The purpose with the test method was to standardise CAF testing. IPC has also published a user guide for CAF testing, IPC-9691, User Guide for the IPC TM-650 Method 2.6.25, Conductive Anodic Filaments (CAF) Resistance Test (Electrochemical Migration Testing) [172].

Two test designs are defined in the test method, IPC-9253 and IPC-9254. They are similar but there are some differences. The two test boards have ten layers and each have four sections

numbered A-D. Sections A and B have test patterns for testing CAF resistance between PTHs and section C has test patterns for testing CAF resistance between PTHs and internal planes. These three sections are common for the two designs. Section D on test board 9253 has test patterns for press-fit compliant pin applications whereas it on test board 9254 has test patterns for layer-to-layer z-axis testing.

When performing the CAF tests, the test boards shall be placed in a humidity chamber and be conditioned in a bias-free state for 24 hours at 23 °C and 50 % RH. After that, insulation resistance measurements shall be made using 100 V DC test voltage. The test is then started by stabilising the test boards for 96 hours at either 65 °C or 85 °C and 87 % RH with no bias applied. Insulation resistance measurements shall then be made oncemore. Any test patterns that have an insulation resistance that is less than 10 Mohm at this time shall be excluded from the test, since that indicates poor hole quality or laminate capability. Then, the bias shall be applied to the test patterns with the same polarity as the test voltage for 500 hours. It is recommended that additional resistance measurements are performed every 24 to 100 hours during the duration of the test, normally 500 hours of applied bias.

See reference 3 for a more extended discussion of test methods and test vehicles for CAF testing.

### 10.5.2 Acceptance criteria

Any drop in resistance for a test pattern by more than one decade in any of the insulation resistance measurements are defined as a failure. For each test pattern, the average of the insulation resistance determined after the initial 96 h exposure to the test conditions in unbiased state is the baseline for the pass-fail criterion.

No acceptance criteria for the CAF test are given in IPC's test method 2.6.25 or in the user guide IPC 9691.

## 10.6 Some thoughts about simulations

**Finite element simulations is** a useful tool to assess how various factors affect reliability of solder joints. However, for several reasons, lead-free soldering has made it more difficult.

### 10.6.1 Anisotropy of tin

It is usually assumed that solder joints have isotropic properties when performing simulations. However, SAC solder joints normally consist of one single tin grain, cyclic twin grains, interlaced twin grains or a mixture of cyclic and interlaced twin grains. The cyclic and interlaced twin grains have only three unique orientations. Since tin grains are highly anisotropic, it may cause effects that simulations assuming isotropic properties cannot predict. For example, the first solder joint to fail may be located more or less randomly under a BGA component. For an isotropic solder, the first solder joints would most likely be located under either the corner of a BGA component or under the corner of an internal chip in the BGA. It is far more difficult to perform simulations for anisotropic solder joints, but it is possible to do simulations to evaluate how anisotropic solder joints affect the fatigue life of the solder joints [96, 106, 107, 122].

### 10.6.2 Changes in material properties of lead-free solders

It is usually assumed that solder joints have constant properties when performing simulations. This was not true even for tin-lead solders since grain coarsening during thermal cycling slightly change the material properties of the solder. However, due to precipitation coarsening in lead-free solders, there is a much larger change in material properties for these solders during thermal cycling. For solder joints with high degree of precipitation hardening, creep may be inhibited until enough precipitation hardening has occurred for facilitation of recrystallisation. Furthermore, the recrystallisation will also change the material properties.

### 10.6.3 Different material properties for interlaced twin structure

LGA components that have solder joints with interlaced structure may have considerably longer fatigue life than solder joints to BGA components despite the much shorter stand-off. That is never observed for components with tin-lead solders. The reason is that lead-free solder joints with interlaced twin structure have different material properties compared to solder joints with single-grained structure or cyclic twin structure. They may also have a different failure mechanism. However, the material properties for interlaced structure have not been determined and, probably, it may vary quite a lot from case to case.

### 10.6.4 Different behaviour of solder joints with mixed CT and IT structure

Since interlaced twin structure has different material properties compared to cyclic twin structure, solder joints with mixed IT and CT structure will have different material properties in the different parts of the solder joints. This will cause faster creep in the part(s) with CT structure. Since the location and the fraction of IT structure in a solder joint with mixed grain structure may vary a lot, the impact of the IT structure may vary from small to very large. Probably, mixed structure might result in some quite early failures, i.e. a low beta value in a Weibull plot.

### 10.6.5 New solders and mixing of solders with different compositions

In the last decade, new lead-free solders have been marketed. They have SAC solder as a basis, but more elements have been added to improve the creep resistance (see section 11.3). Material data are only available for a few of them. Some component manufacturers offer BGA components with solder balls made of these solders, but different solders are used for the components. That is, in many cases, the solder balls and solder pastes used for soldering components will have different solder composition. Depending on the size of the solder balls and the printed amount of solder paste, the composition of the solder in the final solder joints may vary quite a lot. Thus, even if material data are available of the solders used in the solder balls and solder pastes, it will not be available for all the possible compositions in the solder joints.

### 10.6.6 Cracking in PCB laminate and component materials

Due to the higher stiffness of lead-free solders compared to tin-lead solders, there is an increased risk for cracking in the PCB laminate and component materials during thermal cycling. This is difficult to predict from simulations. Also, this is to a large extent also affected by the grain structure and orientations of the grains in SAC solder joints.

# 11. Some results from research projects performed at RISE

## 11.1 Environmental protection provided by conformal coatings

### 11.1.1 Results from evaluations performed in TFP1

The main purpose of conformal coatings is to provide environmental protection against corrosion and electrochemical migration (ECM) on assemblies in harsh field environments. It could be environments where there is a risk for condensation of water on the assemblies and/or where dust or other foreign materials might be deposited on the assemblies.

It is difficult to get good coverage of assemblies with most conformal coatings. It is especially a problem for solvent-based coatings since the dry coating thickness is less than for solventfree coatings. Solvent-free coatings can be applied with larger coating thickness which make it easier to get a better coverage.

Therefore, there is a need to verify that applied conformal coatings provide good environmental protection. As described in section 0, IPC J-STD-001 has only requirements for coating thickness on flat, unencumbered surfaces or on a test coupon. Neither has the standard any requirements that the capability of applied conformal coatings to provide environmental protection is verified.

However, there is a lack of relevant test methods for evaluating the environmental protection provided by conformal coatings. Most test methods used for evaluating the environmental protection provided by conformal coatings are based on measuring surface insulation resistance (SIR) of biased specially designed test boards at controlled temperature and humidity, often at 85 % RH and 85 °C, under a specified time period. These tests are ECM tests and could therefore be expected to be relevant for assessing the environmental protection provided by conformal coatings. The problem is that the test conditions are more benign than the harsh conditions that the product might be exposed to. In fact, if the assemblies have been cleaned prior to application of a conformal coating, an uncoated assembly will normally perform better than coated assemblies because the coating itself has some electrical conductivity. Clearly, such tests do not say anything of the environmental protection provided by a conformal coating.

Since the main purpose of a conformal coating is to preserve the reliability of printed board assemblies used in harsh condition, it is important that tests used to evaluate the environmental protection provided by conformally coated assemblies in harsh conditions are relevant for such evaluations. That is, the test conditions need to be at least as harsh as the field conditions where the product will be used.

Therefore, in TFP1, the environmental protection provided by various conformal coatings were tested using more harsh test conditions. A specially designed test board with test patterns for measuring SIR between solder joints to various types of mounted components were used for the evaluations. The types of components that can be mounted on the test boards include BGA, LGA, QFN, SOIC, QFP, DIL and ceramic capacitors (Figure 40). The test board denoted AP3 is described in reference 9 and the carrying out of evaluations and all test results are presented in reference 10.

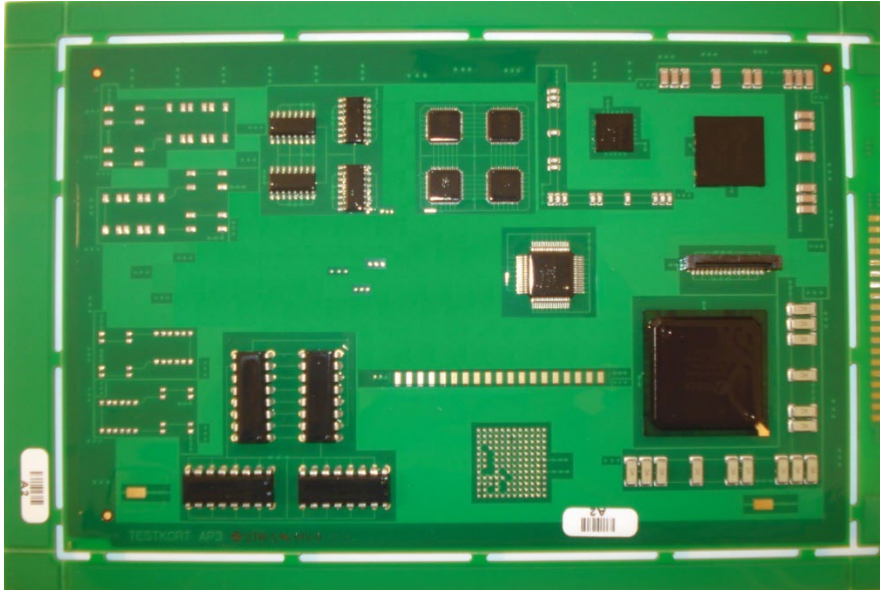


*Figure 40 - Photograph of an assembled test board.*

The test boards were coated with the following five conformal coatings:

- **HumiSeal 1B73EPA**. This is a solvent-based acrylic conformal coating. It contains about 77 % solvent and dries after application. That is, it does not cure after application and can therefore be easily removed with solvents.

- **Tribotec TSE3991CU**. This is a solvent-free silicone conformal coating which is cured by a reaction with water from the humidity in air.

- **Elpeguard SL 1301 ECO-FLZ**. This is a modified polyurethane conformal coating containing about 52 % solvent. It is cured by an oxidative curing reaction with atmospheric oxygen.

- **Parylene C**. This is a coating formed by chemical vapour deposition of chlorinated para-xylylene. This gives a coating with equal thickness on all exposed surfaces.

- **Novec 2708**. This is a fluorinated polymer diluted in a segregated hydro-fluoroether solvent providing a low viscosity, low surface tension coating solution. As for the acrylic coating, it dries and not cures after application.

Since the environmental protection provided by a conformal coating may be degraded by detachment or cracking of the conformal coating, it was decided to use a sequential test programme as described in Figure 41. The assemblies were first exposed to 50 thermal cycles between -40 °C and 100 °C. They were then divided in three groups. The first group went directly after thermal cycling to an ECM test. The second group was exposed to a mixed flowing gas (MFG) test and the third group to salt mist. The second and third groups were then also exposed to the ECM test. After the ECM test, the boards passed through a simulated condensation test.

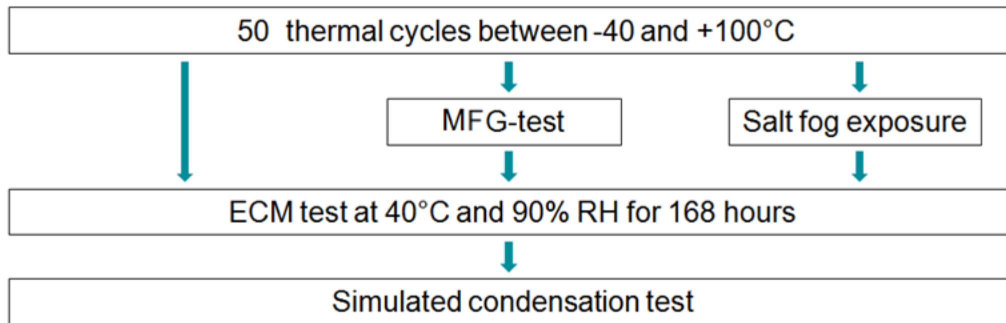



*Figure 41 - Sequential test program used for evaluation of the environmental protection provided by conformal coatings in TFP1.*

The salt fog test and the simulated condensation test have been described in section 0. Besides condensation of water and deposition of foreign material on assemblies, the reliability might be affected by corrosive gases in the field environment. The most common corrosive gases are nitrogen oxides (NO and $NO_2$), sulphur dioxide ($SO_2$), hydrogen sulphide ($H_2S$), chlorine ($Cl_2$) and ammonia ($NH_3$). In ordered to assess the impact of corrosive gases, a mixed flowing gas test was performed according to method 4 in IEC 60068-2-60 [226], but with the concentration of $H_2S$ increased to 100 ppb. The test conditions used in the test are given in Table 12. The test boards were standing unbiased in racks in the test chamber during the exposure to the gases.

Table 12 - *Test conditions during the FMG test.*

| | |
|---|---|
| Gas content of $NO_2$ | 200 ±50 ppb |
| Gas content of $SO_2$ | 200 ±50 ppb |
| Gas content of $H_2S$ | 100 ±10 ppb |
| Gas content of $Cl_2$ | 10 ± 5 ppb |
| Relative humidity | 75 ±3 % RH |
| Temperature | 25 ±1°C |
| Weight gain of reference copper coupons | 1.32 mg/dm$^2$ and day |
| Duration of the test | 21 days |

The ECM test executed in TFP1 was performed basically per IPC-9202 [31]. The test is based on measuring changes in surface insulation resistance (SIR) in humid conditions. Testing was done at 40 °C and 90 % RH for 168 hours. A bias of 5 V DC was applied to the test patterns during the whole test.

Conclusions from this evaluation were:

- Rather little cracking and detachment of the coatings were observed in the thermal cycling test. In a study performed by Taylor and Kinner [227], 1 000 thermal shock cycles were performed between -65 °C to 125 °C to meet automotive requirements. This caused considerable cracking of some of the tested conformal coatings. Therefore, a more “tough” thermal cycling test should perhaps be used if the products will be used in more harsh conditions.

- Although the FMG test provided test conditions that are harsher than experienced in many field conditions, it was not successful in discriminate the capability of the various conformal coatings to provide protection in harsh conditions. Despite the corrosiveness of the gases used in the test, the impact on SIR was very low and no visual corrosion products could be detected even on non-coated boards.

- The results from the ECM test performed on test boards that had not been exposed to FMG or salt fog indicate that testing coated assemblies per IPC-9202 will give very little information about the protection provided by the conformal coatings against electrochemical migration in harsh conditions. In fact, the least degradation of SIR was observed for non-coated boards. This is not surprising since the conditions in the test are milder than the conditions assemblies may be exposed to in harsh field conditions. That is, the test will only show if the coatings themselves may degrade the SIR and/or if contamination such as flux residues present on the board prior to the application of the coatings may cause problem.

- Exposure to salt mist prior to an ECM test or measurement of SIR under simulated condensation of water were shown to be very successful test methods for assessing the protection provided by conformal coatings. Both methods gave similar results and any of them could be used depending on available test equipment.

- Of the tested conformal coatings, only Parylene gave good protection against ECM. The results for this coating were outstanding. It is a different kind of coating which is deposited from a vaporised monomer directly on the surface of the assembly. Thereby, the coting will have the same thickness on all coated surfaces, which will give an outstanding environmental protection. The results for the other coatings varied for different types of evaluated components.

- Besides Parylene, HumiSeal 1B73 gave best protection for area array components, mainly because it gave the best sealing around the components. The protection provided to QFN components and ceramic capacitors was also good, but it was less effective for the components having leads (mainly shown in the simulated condensation test).

- Tribotec TSE3991CU gave poor protection under area array components since its penetration underneath these components was very low. On the other hand, it gave better coverage of the solder joints to many of the other types of components which provided better protection against ECM for these components.

- The results for Elpeguard SL 1301 showed many similarities with the results for HumiSeal 1B73, although the results for a BGA and a QFN were a little inferior.

- Of the tested coatings, Novec 2708 gave the poorest protection against ECM. This is not surprising since it was the thinnest coating.

- The component type that was most difficult to achieve good coverage of wasa QFP component. All coatings except Parylene gave poor protection of the solder joints and leads to this component. Due to the surface tension of coatings before curing, the coatings became very thin at protruding parts and sharp edges which was observed especially at the toes of the leads to the QFP. The protection provided for other leaded components (SOIC and DIL) was also rather poor although not quite as poor as for the QFP. For the smallest ceramic capacitor (0603), the provided protection was also quite poor.

- To really demonstrate that applied conformal coatings provide protection against ECM in harsh conditions, the conditions in a qualification test need tobe at least as harsh as the field conditions.

### 11.1.2 Results from evaluations performed in TFP2

Due to the rather poor environmental protection provided by the conformal coatings evaluated in TFP1 except for Parylene, it was decided to evaluate some more conformal coatings in TFP2. Another reason was that all but the Parylene coating had turned out to have a rather large negative impact on the fatigue life of solder joints to especially BGA and QFN components (see section 11.2.1).

The conformal coatings evaluated in TFP2 were:

- **HumiSeal UV40**. This is a single component, high solids (minimum 95 %), UV curable, acrylated polyurethane conformal coating that possesses excellent chemical resistance, surface hardness, flexibility and moisture resistance. The material is tack free after exposure to UV light. A secondary moisture cure mechanism cures unexposed areas of the coating within 2-3 days at ambient conditions. The solvent content is less than 5 % and the Tg is 45 °C. The coating fluoresces under UV light to allow for coating inspection and can be applied by selective coating equipment.

- **HumiSeal UV500**. This is a high solids (minimum 98 %) UV dual cure elastomeric acrylate conformal coating. It exhibits excellent flexibility, moisture resistance and electrical insulation properties as well as good chemical resistance. The formulation allows chemical stripping using a dedicated stripper. It is tack free after exposure to UV light and the secondary moisture cure mechanism will fully cure any unexposed areas of the coating within 7 days at ambient conditions. The solvent content is less than 2 %

and the Tg is -43 °C. The coating fluoresces under UV light to allow coating inspection and can be applied by all selective coating equipment.

- **HumiSeal 1B73**. This is a solvent-based fast drying acrylic conformal coating. It demonstrates excellent flexibility and electrical properties, fluoresces under UV light for ease of inspection. It contains about 77 % solvent and dries after application. That is, it does not cure after application and can therefore be removed with solvents making repair easy. The Tg is 42 °C.

- **HumiSeal 1A33**. This is a single component, polyurethane conformal coating, suitable for general printed circuit board applications. The solvent content is about 56 % and the Tg is 26 °C. It contains no free isocyanates and fluoresces under UV light for inspection purposes.

- **HumiSeal 1B59NSLU**. This is a fast air drying, single component, synthetic rubber conformal coating that contains methylcyclohexane solvent that is more environmentally friendly than traditional solvents. It has excellent flexibility, low stress on components, extremely low moisture vapor permeability and improved heat resistance. The solvent content is about 78 % and the Tg is 14 °C. The coating demonstrates fluoresces under UV for ease of inspection and is easily repaired.

- **Electrolube 2K301FC**. This is a high performance two-component conformal coating family, designed specifically for selective coating processes. 2K301 is characterised by greater coating thickness and enhanced edge coverage and shows extreme flexibility and extremely low stress on components. It is recommended to be dried at 50-80 °C (80 minutes at 50 °C and 10 minutes at 80 °C). The solvent content is less than 2 % and the Tg is -47 °C.

- **Electrolube 2K850**. This is a rapid LED UV curable, flame retardant, tough yet flexible, high performance two-component, solvent-free conformal coating, designed specifically for selective coating processes. 2K850 is characterised by greater coating thickness and enhanced edge coverage and shows improved adhesion, abrasion, scratch and solvent resistance when compared to conventional single component coatings. The solvent content is less than 1 % and the Tg is -18 °C.

- **Electrolube Expandable Coating**. This is a prototype coating designed to expand by a factor of between 3 and 10 after application, thus ensuring excellent edge coverage, and a very high degree of protective performance, without significantly increasing the weight of protection applied. The low-density coating provides excellent protection against water immersion/condensing environments, mixed flowing gases etc. as well as improved arcing and high voltage performance. The coating has an appearance of a foam and yields very low stress on components.

Basically, the same test board was used in this evaluation as in TFP2, but with some minor modifications [13].

The HumiSeal coatings are also available in gel forms. In order to investigate if the environmental protection provided by UV40, UV500 and 1B73 could be further improved, either the gel form of the coatings or an epoxy glue was applied to the leads to QFP components and on the terminations to ceramic capacitors prior to coating. The epoxy glue used was DELO KATIOBOND 45952 which is a modified UV-cured, one-component epoxy resin. In addition, gels and epoxy glue were applied around the BGA and LGA components on some boards in order to seal around the components to prevent the coatings from penetrating in under the components. The gels and the epoxy glue were in most cases applied prior to the application of the conformal coatings.

Basically, the same sequential test programme was used in TFP2 to evaluate the environmental protection provided by the conformal coatings as in TFP1, but with some modifications. The number of thermal cycles were increased to 200 cycles, the temperature cycles were performed between -40 °C and 85 °C and the MFG test was deleted.

The execution of the evaluations and all test results are presented in reference 14.

Conclusions from this second evaluation were:

- HumiSeal 1B59, Electrolube 2K301 and the Electrolube Expandable coating provided the best environmental protection followed by HumiSeal 1B73.
- HumiSeal UV40 provided good environmental protection when tested without prior exposure to salt mist, but the environmental protection was rather poor if exposed to salt mist prior to humidity testing.
- Although the environmental protection provided with HumiSeal UV500 was inferior to HumiSeal UV40 when tested without prior exposure to salt mist, its performance was superior to HumiSeal UV40 if exposed to salt mist prior to humidity testing.
- The material itself in Electrolube 2K850 appeared to cause degraded SIR. Furthermore, considering the large thickness of the coating, it did not provide very good environmental protection.
- Application of coating gel or epoxy glue on solder joints to ceramic capacitors or leads to a QFP component did not improve the environmental protection. In fact, it deteriorated the environmental protection in some cases due to extensive cracking. However, when applied around area array components prior to coating, it improved the environmental protection.
- As for Electrolube 2K850, the material itself in the epoxy glue applied on solder joints and around area array components seem to degrade SIR. Furthermore, it did not seem to improve the environmental protection.

## 11.2 Impact of conformal coatings and underfills on solder joint fatigue

### 11.2.1 Results from evaluations performed in TFP1

A risk with using a conformal coating is that it may shorten the fatigue life of solder joints if it completely or locally fills the space underneath components. Therefore, the impact of four conformal coatings on the fatigue life of solder joints to various types of components were evaluated in TFP1. In addition, the impact of two underfills was also evaluated. A specially designed test board was used for this. It was a 6-layer PCB with ENIG as surface finish. It was mounted with BGA, WLP, LGA, QFN, ceramic resistors, chip array resistors and MELF components. The design of the test board and how test boards were manufactured are described in more detail in reference 4.

The evaluated conformal coatings were:

- **HumiSeal 1B73EPA**. This is a solvent-based acrylic conformal coating. It contains about 77 % solvent and dries after the application. That is, it does not cure after application and can therefore be easily removed using organic solvents.
- **HumiSeal UV500**. This is a solvent-free UV curable, single-component, elastomeric acrylate coating. It has a secondary moisture cure mechanism for curing in non-UV exposed areas.
- **Tribotec TSE3991CU**. This is a solvent-free silicone conformal coating which is cured by a reaction with humidity from the air.
- **Parylene C**. This is a coating formed by chemical vapour deposition of para-xylylene. The coating process gives a coating with equal thickness on all exposed surfaces.

Before applying the coatings, about half of the boards were cleaned using Vigon US as cleaning agent in a Kerry batch cleaning equipment using immersion spray. Except for Parylene, the coatings were applied by companies participating in the project using their ordinary processes for coating assemblies with coating robots. The thicknesses of the coatings on flat surfaces were about 30 µm for HumiSeal 1B73, about 90 µm for HumiSeal UV500 and about 150 µm for Tribotec TSE3991. An extra cleaning was done prior to the application of Parylene. This cleaning was done with isopropanol and light brushing followed by drying. The thickness of the applied Parylene coating was about 15 µm.

The evaluated underfills were:

- **ECCOBOND E 1216M**: This is an epoxy fast-flowing capillary underfill encapsulant with a $T_g$ of 125 °C and a storage modulus of 4.05 GPa at 25 °C. The CTE is 35 ppm/°C below $T_g$ and 131 ppm/°C above $T_g$.
- **ECCOBOND E 1172A**: This is an epoxy fast-flowing capillary underfill encapsulant with a $T_g$ of 135 °C and a flexural modulus of 8.6 GPa at 25 °C. The CTE is 27 ppm/°C below $T_g$ and 85 ppm/°C above $T_g$.

Underfill were applied underneath the following components:

- BGA208 with 0.8 mm pitch
- CTBGA132 with 0.5 mm pitch,
- WLP16 with 0.4 mm pitch,
- LGA133 with 1.27 mm pitch.
- MLF72 with 0.5 mm pitch.
- Ceramic resistor 2010
- Chip array resistor 1206
- MELF2308

For the area array components, the underfills were applied on two adjoining sides and was then allowed to fill the space underneath the components by capillary forces. For MLF72, they were applied on all sides and for passive components on two sides. The underfills were applied both on assemblies that had been cleaned prior to the application and to assemblies that had not been cleaned.

The impact of the conformal coatings and the underfills on the fatigue lives of solder joints to the various components were evaluated by thermally cycling the test boards between -40 °C and 100 °C with temperature ramps of 10 °C/min. The dwell time was 10 min at $T_{min}$ and 30 min at $T_{max}$. The test was stopped after 6121 cycles had been performed. The test setup, the execution of the evaluation and the test results are reported in detail in reference 8.

Two-parameter Weibull plots were performed to determine the characteristic fatigue life of the solder joints to the various components. From the Weibull plots, the characteristic fatigue life (eta value) and the shape parameter (beta value) were calculated.

The results from the testing are summarised in a bar chart shown in Figure 42.

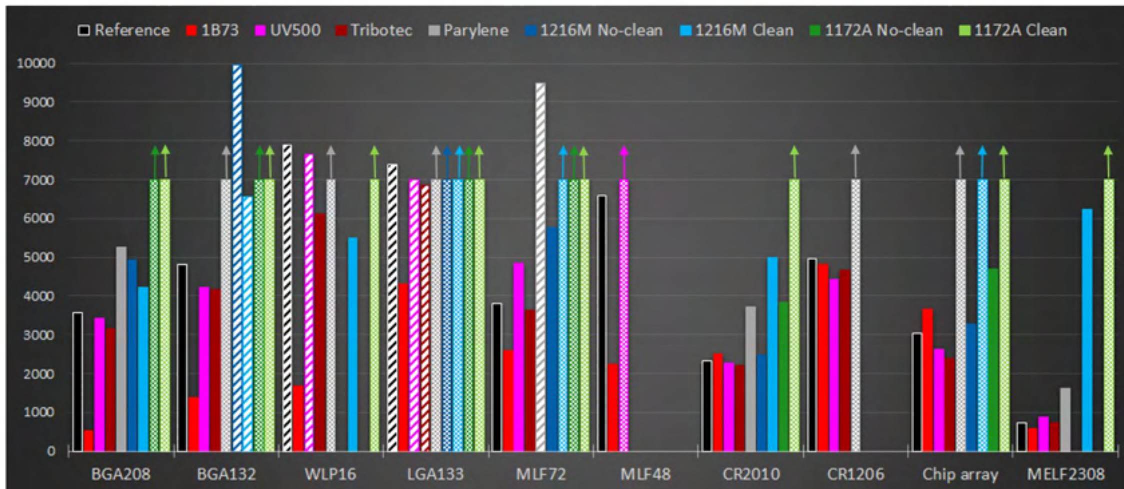



*Figure 42 - Bar chart showing the eta values for the various tested components. Reference is non-coated assemblies. Striped bars indicate uncertain values due to few failures whereas spotted bars indicate that no failures had occurred after 6 151 cycles, i.e. the eta values ought to be considerably higher than 7 000 cycles.*

The following conclusions were drawn from the evaluation:

- Different types of conformal coatings may have very different impact on the fatigue life of solder joints.
- The Parylene coating, with a thickness of 15 µm, increased the fatigue life of solder joints to the various types of components with 50-200 %.
- HumiSeal 1B73 decreased the fatigue life of solder joints to area array components with 50-90 % and to MLF components with 30-65 %. Likely, this was caused by coating material penetrating in under the components and at some locations entirely filling the space causing large stress on the solder joints during thermal cycling. This behaviour is probably most accentuated for acrylic conformal coatings.
- HumiSeal UV500 and Tribotec had no significant impact on the fatigue life of solder joints, probably because these coating materials did not penetrate in under the area array and MLF components.
- Cleaning prior to conformal coating had no significant impact on the fatigue life of solder joints to components coated with HumiSeal UV500 and Tribotec, but it did affect the fatigue life for components coated with HumiSeal 1B73. For most component types, cleaning prior to coating with HumiSeal 1B73 degraded the fatigue life of the solder joints, whereas it for a few component types had no effect or even improved the fatigue life.
- An underfill may cause a large improvement of the fatigue life of solder joints, not only to area array components but to all types of components, but the properties of the underfill is important for how much the fatigue life is improved.

- The improvement of the fatigue life by underfill 1216M was for most components rather low. In fact, for a WLP component it even caused a reduction of the fatigue life.
- The results for components underfilled with 1172A were outstanding, i.e. the underfill with the lowest CTE and the highest modulus. Of the components underfilled with 1172A, failures were only registered for some passive components on non-cleaned assemblies.
- Cleaning prior to the application of underfills improved the fatigue life of the solder joints in most cases, but for some components it degraded the fatigue life. This was especially the case for underfill 1216M.

### 11.2.2 Results from evaluations performed in TFP2

Due to the large negative impact on the fatigue life of solder joints by all conformal coatings evaluated in TFP1 except Parylene, it was decided to evaluate additional coatings in TFP2. It was also due to the poor capability of coatings evaluated in TFP1 (except for Parylene) to provide environmental protection of leads to leaded components and of terminations to ceramic capacitors. One of the objectives in TFP2 was to find coatings that provides good environmental protection without a negative impact on the fatigue life of solder joints.

Furthermore, it is quite costly to apply underfills under components. Materials that will flow underneath the components due to capillary forces are very expensive, they need to be transported and stored at very low temperatures, and they need advanced manufacturing processes for applying the materials. An alternative and cheaper method is to apply underfills only at the corners or edges of components. These materials will only partly flow under the components. Therefore, it was decided to evaluate also such a material.

A new test board was designed for this evaluation. It was a 10-layer HDI board with 2+6b+2 stackup and with ENIG as surface finish. It was mounted with BGA, WLP, a-CSP (a kind of WLP component), MLF, ceramic resistors and MELF components. The design of the test board and how test boards were manufactured are described in detail in reference 13.

In TFP2, the following five conformal coatings were evaluated: Electrolube 2K301FC, HumiSeal1A33, Electrolube Expandable Coating, HumiSeal 1B59NSLU and HumiSeal 1B73. They have been described in section 11.1.2

Except for HumiSeal 1A33, the test boards were not cleaned prior to the application of the conformal coatings. The boards coated with HumiSeal 1A33 were cleaned with Zestron FA as cleaning agent prior to the application of the coating.

ECCOBOND E 1172A was included also in this study. In addition to this underfill, two newunderfills were also evaluated. These were:

- **ECCOBOND UF 1173.** This is an epoxy based, single component underfill with a $T_g$ of 160 °C and a flexural modulus of 5.9 GPa at 25 °C. The CTE is 26 ppm/°C below $T_g$ and 103 ppm/°C above $T_g$.
- **ECCOBOND EO 1072.** This underfill has a rheology that allows the same product to be used as both a dam and fill encapsulant with a $T_g$ of 135 °C and a flexural modulus of 6.7 GPa at 25 °C. The CTE is 43 ppm/°C below $T_g$ and 123 ppm/°C above $T_g$.

Underfill UF 1173 was applied on both non-cleaned and cleaned test boards whereas the two other underfills were only applied on non-cleaned test boards.

Underfills E1172A and UF1173 were applied underneath all components. For the BGA, a-CSP and WLP components, the underfills were applied on two adjoining sides and was then allowed to fill the space underneath the components by capillary forces. For the MLF components, the underfills were applied on all sides and for the MELF and for ceramic resistors on two sides.

Underfill EO1072 was applied in the four corners of the BGA, a-CSP, WLP and MLF components and on the two sides of the MELF and ceramic resistors.

The assemblies were thermally cycled between -40 °C and 125 °C with temperature ramps of 10 °C/min. The dwell time was 10 min at $T_{min}$ and 30 min at $T_{max}$. The test was stopped after 4 300 cycles had been completed. The results from the testing are presented in Figure .

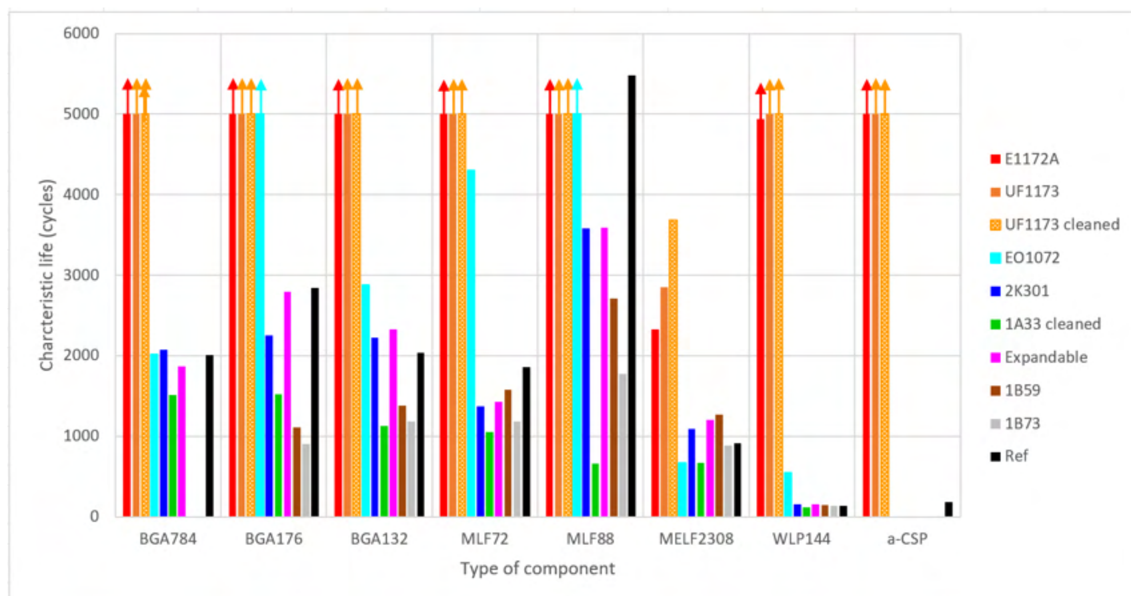



*Figure 43 - Bar chart showing eta values for the various components. Arrows above bars indicate that too few failures have occurred to determine the characteristic life and that they can be expected to be considerably higher than the bars imply.*

The following conclusions were drawn from this study:

- Underfills E1172A and UF1173 provided a very large improvement of the fatigue life of solder joints, not only for area array components but also for MLF and passive components. For components such as a-CSP and WLP144, which have a very short fatigue life, it may be necessary to apply underfills to provide long enough fatigue life of the solder joints in harsh conditions.

- Underfill EO1072 applied to corners of components improved the fatigue life of solder joints to most components, but not all. For components where the solder joints most likely to fail are located far from the corners, EO1072 applied to the corners did not improve the fatigue life. Furthermore, it may have a negative effect on the reliability of PTHs located underneath BGA components.

- Conformal coatings Expandable and 2K301 had no or only a small negative impact on the fatigue life of the solder joints to the area array components, but they degraded the fatigue life of solder joints to MLF components with 25-35%.

- The HumiSeal coatings degraded the eta values with 30-70% for most of the components. Of the three HumiSeal coatings, 1B59 performed best followed by 1B73.

- When combining the results from this part of the study with the results from the part of the study in which the environmental protection provided by the conformal coatings was evaluated, the Expandable coating and 2K301 provided the best environmental protection in harsh conditions and the least negative impact on the fatigue life of solder joints to various types of components. Coating 1B59 provided good environmental protection but had a larger negative impact on the fatigue life of solder joints than the former coatings. The environmental protection provided by 1B73 and 1A33 was not as good as for the other coatings and they had a little more negative impact on the fatigue life of solder joints.

## 11.3 Impact of high reliability solders on solder joint fatigue

**During the past 10 years,** new solders have been developed that are claimed to be more creep resistant than common SAC solders**.** Therefore, they are claimed to provide a longer fatigue life of solder joints but also that they can be used in products with higher operating temperatures of 150-175 °C.

The improved creep resistance of the new solders has been achieved by adding more elements to common lead-free solders based on tin, silver and copper. The most common additives are bismuth (Bi), antimony (Sb), indium (In) and Ni (Ni). These elements enhance the precipitation hardening of the solders but provide also solid solution hardening. This makes them more creep resistant. They are often called “high reliability solders - HRS” or “high performance solders”.

Three such solders were evaluated in TFP2. A specially designed test board that could be mounted with different types of components was designed for the evaluations [13]. The

component types included area array components, QFN components and passive components. All but one of the area array components had solder balls consisting of SAC solder. The exempted BGA component had solder balls consisting of SACQ, an HRS with the composition Sn4.0Ag0.5Cu3.0Bi0.05Ni.

The components were soldered using solder pastes with the three HRS alloys and their impact on the reliability of solder joints to the various types of components were compared with components soldered with SAC305 and SnPb solder pastes. The evaluated HRS alloys were Innolot, SB6NX and Indalloy 292 with compositions and melting ranges given in Table 13.

Table 13 - *Elemental composition of tested solder given as weight-% and melting ranges.*

| Solder paste | Sn | Ag | Cu | Bi | Sb | In | Ni | Pb | Melting range |
|---|---|---|---|---|---|---|---|---|---|
| Innolot | 91.0 | 3.8 | 0.7 | 3.0 | 1.4 | - | 0.15 | - | 206-218 °C |
| SB6NX | 89.2 | 3.5 | 0.8 | 0.5 | - | 6.0 | - | - | 202-206 °C |
| Indalloy 292 | 86.7 | 3.2 | 0.7 | 3.2 | 5.5 | 0.5 | 0.2 | - | 214-229 °C |
| SAC305 | 96.5 | 3.0 | 0.5 | - | - | - | - | - | 217-221 °C |
| Sn62Ag36Pb | 62.0 | 2.0 | - | - | - | - | - | 36.0 | 178-180 °C |

The impact of the choice of PCB laminate, PCB stack-up and surface finish on PCB pads on the fatigue lives of the solder joints were also evaluated.

The fatigue lives of the solder joints to the various components were evaluated by performing thermal cycling between -40 °C and 85 °C (TC1) and between -40 °C and 125 °C (TC2).

All results from the evaluations are presented in reference 14. The following conclusions were drawn from the evaluations:

Using solder pastes based on "high reliability solder alloys" to solder area array components with SAC305 solder balls can to some extent both improve and degrade solder joint fatigue lives compared to solder pastes based on SAC305. The outcome may depend on the composition of the solder. In this investigation, SB6NX generally performed a little better than both Innolot and Indalloy, but the difference in performance was not large. Solder volume in the solder joints as well as surface finishes on the solder pads on both the PCB and the component may also affect solder joint fatigue differently depending on the solder alloy composition. However, it is difficult to predict how a change of any of these factors will affect the fatigue of solder joints to a specific component.

Replacing SAC305 solder balls on area array components with “high reliability solder” balls may improve the fatigue lives of the solder joints considerably. Since only one type of component having “high reliability solder” balls has been tested in this study, and it differed

in several aspects from the same component with SAC305 solder balls, it is not possible to postulate that “high reliability solder” balls will always improve the fatigue life for all area array components.

If area array components having SAC305 solder balls are soldered using SnPb solder paste and a soldering profile for SnPb soldering, but with a top temperature of 230 °C, the solder balls will be completely remelted during soldering. The fatigue life of such components will be as good as or better than for components soldered with Innolot or SAC305.

Although the results for MLF components at a first glance indicated that all “high reliability solders” improved the fatigue lives of the solder joints, the results may instead be due to a larger stand-off of the components soldered with these solders. However, it cannot be ruled out that the high reliability solders, and particularly Indalloy 292, may have improved the fatigue life of the solder joints of MLF components to some extent.

The results for MELF components varied. The results show a very large improvement of the fatigue life for components soldered with Indalloy 292 and Innolot compared to SAC305, but no improvement for components soldered with SB6NX.

Too few failures occurred for ceramic resistors to make it possible to judge how the different solders affected the fatigue life of the solder joints to these components.

Cracks were formed in the PCB laminate to a large extent in test TC2, but also in the substrate of BGA176. These cracks improve the fatigue lives of solder joints since they reduce the stress on the solder joints during thermal cycling. Therefore, if cracks form in the PCB laminate or in BGA substrates during thermal cycling, they may cause a large overestimation of the fatigue life of solder joints under field conditions where cracks will not form. Therefore, if it shall be possible to use high reliability solders at field temperatures of 150-175 °C, it would require other types of PCBs to avoid very extensive cracking in the PCB, but also other types of sub-strates in some BGA components.

High density interconnect (HDI) boards were more susceptible to cracking in the PCB laminated than standard boards.

Due to the extensive cracking in PCB laminates and BGA substrates in TC2, the maximum temperature in accelerated thermal cycling test should preferably not be higher than 85 °C unless the temperature will be higher under field conditions. Although cracks also formed in test TC1, the extent of cracking in the PCB laminate was very low.

Most of the tested component had fatigue lives that will meet requirements for most applications. However, the fatigue life of solder joints to the a-CSP and WLP144 will be too short for products used in harsh conditions.

In conclusion, the results from the evaluation did not indicate any significant improvement in fatigue life of solder joints to BGA components with SAC solder balls and QFN components by using high reliability solders. They may improve the fatigue life of solder joints to passive components and also to BGA components if they have HRS balls.

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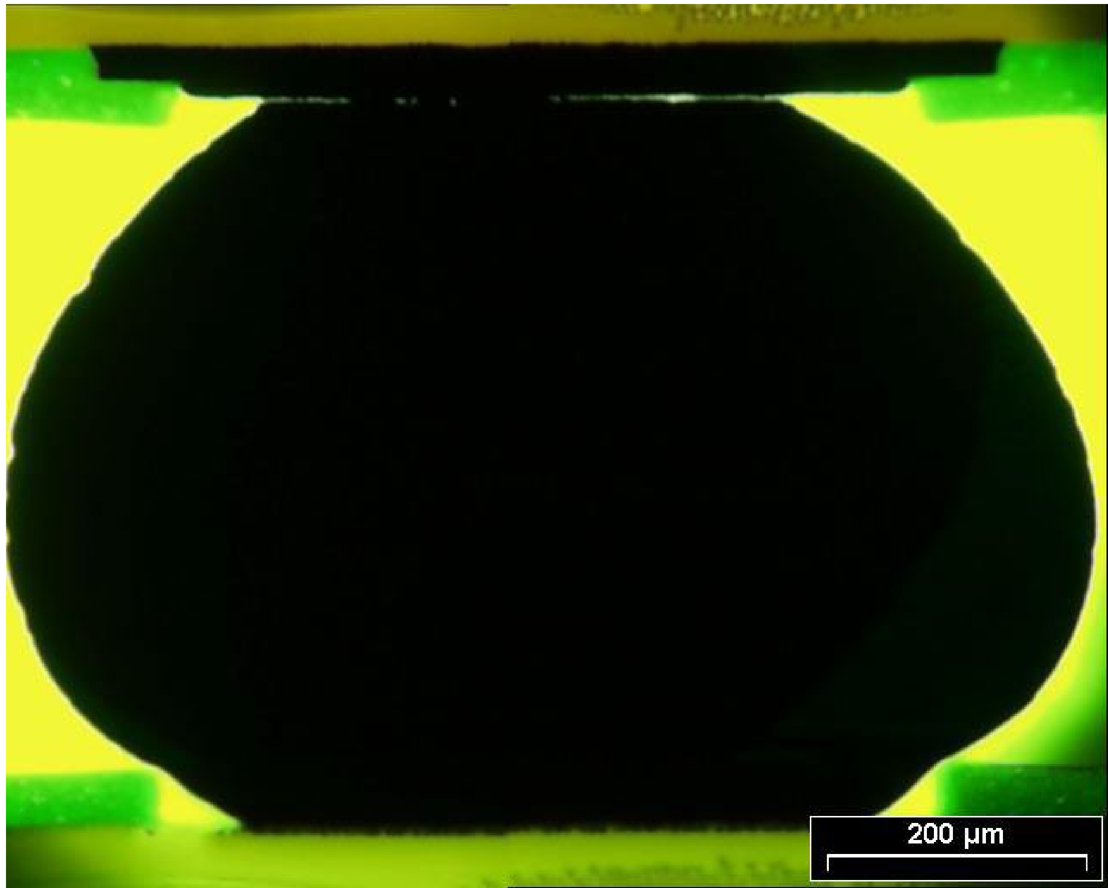
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